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PATENT ABSTRACTS OF JAPAN

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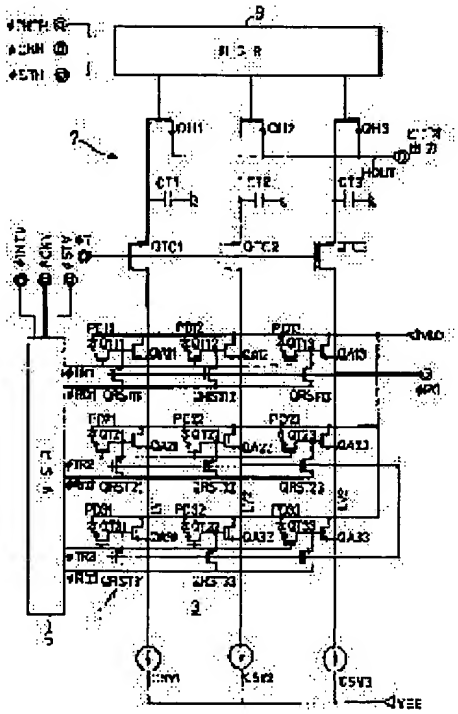
(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent an excess rush current caused when all picture elements of the solid-state image pickup device are reset.

SOLUTION: The solid-state image pickup device having plural pixels for photoelectric conversion and scanning circuits 5, 9 selecting sequentially the plural picture elements 1 is provided with a shift register as a scanning circuit to set outputs of plural circuit stages to a prescribed logic state nearly simultaneously and with a light receiving element PD as a picture element 1 and an amplifier element QA amplifying a signal charge stored in the light receiving element PD. Outputs of plural circuit stages of the shift register of the scanning circuit 5 are set to the prescribed logic state to select plural picture elements 1 and the charge of the light receiving element PD is reset while the plural selected picture elements 1 cut off the amplifier element QA.



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CLAIMS

[Claim(s)]
[Claim 1] Two or more pixels which perform photo electric translation. The scanning circuit for choosing two or more aforementioned pixels one by one, and reading them. It is the solid state camera equipped with the above. the aforementioned scanning circuit Continuation connection is made, two or more circuit stages are constituted, and it has the shift register which can be set as a predetermined logic state almost simultaneous for the output of two or more aforementioned circuit stages according to the input of a predetermined control signal. The photo detector to which the aforementioned pixel accumulates the signal charge according to the lightwave signal at least respectively, While choosing two or more pixels by having the amplifier which amplifies the signal charge accumulated at this photo detector, and setting the output of two or more circuit stages of the shift register of the aforementioned scanning circuit as the aforementioned predetermined logic state It is characterized by reducing the rushes current at the time of reset by resetting the charge of the aforementioned photo detector, where the aforementioned amplifier is cut off in two or more selected pixels.
[Claim 2] the solid state camera according to claim 1 characterized by for the pixel of each above possessing the transfer element which transmits further the signal charge accumulated at the aforementioned photo detector to the control electrode of the aforementioned amplifier, and the reset element which resets the charge of the control electrode of the aforementioned amplifier, and resetting the charge of a photo detector by setting both the aforementioned transfer element and the aforementioned reset element to ON
[Claim 3] Furthermore, the solid state camera according to claim 2 characterized by including the bias voltage impression means for impressing bias voltage to the aforementioned amplifier and holding the aforementioned amplifier in the cut-off state in case the charge of a photo detector is reset by setting both the aforementioned transfer element and a reset element to ON.
[Claim 4] Two or more pixels which consist of an amplified type photo-electric-translation means to be arranged in the shape of two-dimensional, and to accumulate and amplify the signal charge according to the lightwave signal respectively in a line and the direction of a train. The current regulator circuit prepared for each [which connected in common the output terminal of each pixel arranged in the direction of a train] train line of every, and horizontal and perpendicular each scanning circuit which carries out the selection drive of the aforementioned pixel. Are the solid state camera equipped with the above, and continuation connection is made, two or more circuit stages are constituted, and the aforementioned vertical-scanning circuit is equipped with the shift register which can be set as a predetermined logic state for the output of two or more aforementioned circuit stages almost simultaneous according to the input of a predetermined control signal. The photo detector which accumulates the signal charge [pixel / aforementioned] corresponding to the lightwave signal respectively, and the amplifier which amplifies the signal charge accumulated at this photo detector, The transfer element which transmits the signal charge accumulated at the aforementioned photo detector to the control electrode of the aforementioned amplifier, The reset element which resets the charge of the control electrode of the aforementioned amplifier is provided. The control electrode of the transfer

element of the pixel of each line is connected to the line line which corresponds in common. The line line of each line is connected to the correspondence circuit stage of the aforementioned vertical-scanning circuit, and the control electrode of the reset element of all pixels is connected to a reset control signal input terminal in common. And all transfer elements are set to ON through each aforementioned line line by setting the output of two or more circuit stages of the shift register of the aforementioned vertical-scanning circuit as the aforementioned predetermined logic state. And while setting the reset element of all pixels to ON and resetting the charge of a photo detector through a transfer element and a reset element by adding the aforementioned reset control signal to the reset element of all pixels By impressing the voltage which makes this amplifier a cut-off state through the reset element which was turned on on the occasion of this reset at the control electrode of an amplifier, it is characterized by reducing the rushes current at the time of reset.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Concerning a solid state camera, this invention is used for an electronic still camera etc., and instant-reset of all pixels is possible for it, and it relates to the solid state camera which can moreover reduce the rushes current at the time of reset sharply.
[0002]
[Description of the Prior Art] Drawing 6 shows the composition of the outline of the conventional solid state camera, and shows the example of two-dimensional image sensors. The equipment of this drawing is considered as the pixel composition of three line x3 train for simplification of explanation. Moreover, although the subscript is given to the reference mark of each element in the drawing, a subscript may be omitted when expressing on behalf of the element of the same kind for simplification of explanation.
[0003] With the equipment of drawing 6 , the static induction transistor (SIT) is used as an example of an amplified type photo detector as each pixel. That is, the static inductions transistor QS11, QS12, QS13, QS21, QS22, QS23, QS31, QS32, and QS33 which constitute each pixel are arranged in the shape of [of three line x3 train] a matrix.
[0004] Moreover, the vertical-scanning circuit VSR for choosing the pixel of each train one by one for every line is formed. That is, the gate of the static induction transistor arranged among the pixels arranged in the shape of a matrix at each line writing direction is connected to each circuit stage of the shift register of the vertical-scanning circuit VSR through each line line GV1, GV2, and GV3 in common. For example, the gate of static inductions transistor QS11, QS12, and QS13 is connected to the vertical-scanning circuit VSR through both the line lines GV1, and the gate of each static inductions transistor QS21, QS22, and QS23 is connected to the vertical-scanning circuit VSR through the line line GV2. All circuit stages are reset or preset by impression of initialization signal phiINTV, and the vertical-scanning circuit VSR can change all the line lines GV1, GV2, and GV3 into the selection state by it.
[0005] Moreover, the source of the static induction transistor of the pixel of each train is connected common to the train lines LV1, LV2, and LV3 of the train, and each train line is connected to the predetermined power supply VEE through the constant current source CSV. Each constant current source CSV serves as a load of the static induction transistor QS of each pixel at the time of signal read-out from each pixel. The drain of the static induction transistor QS of each pixel is connected to the predetermined power supply VDD in common. The end of each train lines LV1, LV2, and LV3 is grounded through the transistors QRSTV1, QRSTV2, and QRSTV3 for perpendicular reset for resetting each train line. Reset-signal phiRSTV for perpendicular read-out lines explained later is supplied to each transistor for perpendicular reset.
[0006] The other end of each train lines LV1, LV2, and LV3 is connected to the drain of each transistor QH1, QH2, and QH3 for a level output through each switch QT1, QT2, and QT3 for a transfer. The source of each transistor for a level output is connected to the common level output line HOUT, and this level output line HOUT is connected to the video outlet terminal for supplying an image pck-up signal

outside. Moreover, the source of each transistors QT1, QT2, and QT3 for a transfer is grounded through each capacity CT1, CT2, and CT3.
[0007] The gate of the transistors QT1, QT2, and QT3 for a transfer of each train is connected in common, and transfer pulse phiT is supplied. Moreover, the gate of the level read-out transistors QH1-QH3 is connected to each circuit stage of the horizontal scanning circuit HSR. Like [the horizontal scanning circuit HSR] the aforementioned vertical-scanning circuit VSR, it has a shift register and, as for this shift register, the thing in which the set or reset of all circuit stages is possible is used by level initialization signal phiINTH.
[0008] When used for example, for an electronic still camera, the solid state camera of drawing 6 operates by adding perpendicular start signal phiSTV to the vertical-scanning circuit VSR, and adding clock signal phiCKV for a perpendicular shift after progress of the predetermined exposure time, so that the shift register of the vertical-scanning circuit VSR may shift the aforementioned start signal phiSTV to each circuit stage one by one. Each line lines GV1, GV2, and GV3 are chosen one by one by this. The signal charge according to the incident light is accumulated at each static induction transistor QS, and the voltage corresponding to the charge by which this static induction transistor operated as a source follower, and was accumulated is outputted to each train line LV by applying predetermined selection voltage to the gate voltage in the selected line. That is, the signal from the static induction transistor QS of the selected line is simultaneously outputted to each perpendicular read-out line LV.
[0009] And after making it flow through the transfer transistor QT of each train by transfer signal phiT at this time and charging a signal charge at capacity CT1, CT2, and CT3, QT is intercepted, and the signal for every train is outputted to the level output line HOUT by setting the level read-out transistor QH to ON one by one by the vertical-scanning circuit HSR.
[0010] By the way, when such a solid state camera is used for example, for an electronic still camera, after resetting all pixels at the moment of pushing a shutter, the image pck-up of a photographic subject picture is performed. In the solid state camera of drawing 6 , reset of all pixels is performed as follows.
[0011] That is, the vertical-scanning circuit VSR is controlled by initialization signal phiINTV, clock signal phiCKV, and scanning start signal phiSTV including a shift register. If initialization signal phiINTV and phiSTV are made into highness, all the circuit stages of the vertical-scanning circuit VSR are preset, all the line lines GV1, GV2, and GV3 become highness, and all pixels will be in a selection state. On the other hand, if initialization signal phiINTV is made into highness and scanning start signal phiSTV is made into a low, each circuit stage of the vertical-scanning circuit VSR is reset, and all pixels will be in the state where it does not choose. If initialization signal phiINTV is made into a low, the vertical-scanning circuit VSR will start the usual shift operation, whenever clock signal phiCKV enters from the time of start signal phiSTV becoming highness, each line lines GV1, GV2, and GV3 serve as a high level one by one, and the pixel of one line is chosen at a time one by one.
[0012] And in order to reset all pixels in the solid state camera of drawing 6 , reset-signal phiRSTV only for perpendicular read-out is first made into highness, the transistors 1-QRSTV 3 for perpendicular reset of each train are set to ON, and each train lines LV1, LV2, and LV3 are connected to a gland.
[0013] Next, both aforementioned initialization signal phiINTV of the vertical-scanning circuit VSR and scanning start signal phiSTV are made into highness, and each circuit stage of the vertical-scanning circuit VSR is changed into a presetting state. By this, each line lines GV1, GV2, and GV3 of both become high-level, and will be in the selection state of all pixels. The high-level voltage of each line lines GV1, GV2, and GV3 in this case, i.e., the voltage of control signal phiSRs 1-3, is set up so that it may become the voltage VRSTP for reset of static inductions transistor 11-QS 33.
[0014] As everyone knows, an inversion layer is formed in the gate electrode lower part of each static inductions transistor QS11-QS33, a channel is made between the source drains of these static inductions transistor 11-QS 33, the residual charge charged at the gate flows out, and reset of all pixels is performed by this. At this time, the current by the outflow of the residual charge by reset flows simultaneously to the static inductions transistor QS11-QS33 of each pixel.
[0015]
[Problem(s) to be Solved by the Invention] Thus, in the solid state camera which has the conventional

amplified type image pck-up element, when all pixels were reset, it was resetting by making the pixel section including an amplification means into one by choosing all pixels simultaneously. For this reason, at the time of reset, all the amplification meanses in each pixel are also turned on [them] simultaneously, and the current of all amplification meanses flows all at once. Although the current at this time is called rushes current, since all pixels are it turned on that the rushes current of each pixel is small simultaneously, big rushes current flows with the whole image pck-up equipment.
[0016] For example, though the rushes current of each pixel is a number microampere, when the number of pixels is 1 million pixels, with the whole image pck-up equipment, it amounts to several A. When the current which reaches in the chip of a solid state camera at several A flowed, there was also a possibility of the fall of the reliability by electromigration becoming a problem, and the voltage of each [in a chip] portion having not fitted in the predetermined voltage range with the parasitism impedance of each portion in a chip, and the performance which the chip expected as a solid state camera not having been demonstrated, or producing the malfunction by rushes current etc.
[0017] Therefore, the purpose of this invention is to enable it to also prevent the fall of the reliability of a solid state camera exactly while the excessive rushes current at the time of reset is prevented in the solid state camera which used the amplified type pixel and the whole chip of a solid state camera enables it to demonstrate a predetermined performance in view of the trouble in such conventional equipment.
[0018]
[Means for Solving the Problem] In the solid state camera possessing the scanning circuit for according to the 1st **** of this invention, choosing two or more pixels which perform photo electric translation, and two or more aforementioned pixels one by one, and reading them, in order to attain the above-mentioned purpose Continuation connection of two or more circuit stages should be made, and the aforementioned scanning circuit should be constituted, and should be equipped with the shift register which can be set as a predetermined logic state for the output of two or more aforementioned circuit stages almost simultaneous according to the input of a predetermined control signal. The photo detector to which the aforementioned pixel accumulates the signal charge according to the lightwave signal at least respectively, While choosing two or more pixels by having had the amplifier which amplifies the signal charge accumulated at this photo detector, and setting the output of two or more circuit stages of the shift register of the aforementioned scanning circuit as the aforementioned predetermined logic state The rushes current at the time of reset is reduced by resetting the charge of the aforementioned photo detector, where the aforementioned amplifier is cut off in two or more selected pixels.
[0019] With such composition, where the aforementioned amplifier is cut off in two or more pixels which chose and chose two or more pixels with the shift register of the aforementioned scanning circuit, the charge of the aforementioned photo detector is reset. Therefore, it is lost that rushes current flows to an amplifier at the time of reset, and it is lost that excessive rushes current flows though all the pixels in the solid state camera which has many pixels are reset simultaneously. Therefore, it becomes without the reliability of a solid state camera not falling and moreover the voltage of each portion in the chip of a solid state camera causing a big change by rushes current, and a solid state camera can demonstrate an original performance now exactly.
[0020] in this case, the pixel of each above shall possess the transfer element which transmits further the signal charge accumulated at the aforementioned photo detector to the control electrode of the aforementioned amplifier, and the reset element which resets the charge of the control electrode of the aforementioned amplifier, and shall reset the charge of a photo detector by setting both the aforementioned transfer element and the aforementioned reset element to ON
[0021] By taking such pixel composition, it becomes possible to emit the charge accumulated at the photo detector through the aforementioned transfer element and a reset element, where an amplifier is cut off by applying the voltage which sets the aforementioned transfer element and a reset element to ON at both the times of reset, and cuts off this amplifier to the control electrode of an amplifier through a reset element.
[0022] Furthermore, in case the charge of a photo detector is reset by setting both the aforementioned transfer element and a reset element to ON, it can also constitute so that the bias voltage impression

means for impressing bias voltage to the aforementioned amplifier and holding the aforementioned amplifier in the cut-off state may be included.

[0023] In this case, the bias voltage for changing the aforementioned amplifier into a cut-off state to the aforementioned amplifier at the time of reset of a pixel by the above-mentioned bias voltage impression means can be impressed. Therefore, the property of a photo detector and an amplifier can be set as the independently optimal respectively thing, where an amplifier is cut off completely, perfect depletion-ization of a photo detector can be attained, the flexibility of a design of each element increases, and a quality solid state camera can be realized.

[0024] Moreover, two or more pixels which consist of an amplified type photo-electric-translation means to be arranged in the shape of two-dimensional, and to accumulate and amplify the signal charge according to the lightwave signal respectively in a line and the direction of a train in other **** of this invention, In the current regulator circuit prepared for each [which connected in common the output terminal of each pixel arranged in the direction of a train] train line of every, and the solid state camera which carries out the selection drive of the aforementioned pixel and which has level and perpendicular each scanning circuit Continuation connection of two or more circuit stages should be made, and the aforementioned vertical-scanning circuit should be constituted, and should be equipped with the shift register which can be set as a predetermined logic state for the output of two or more aforementioned circuit stages almost simultaneous according to the input of a predetermined control signal. The aforementioned pixel respectively the signal charge according to the lightwave signal The photo detector to accumulate, the amplifier which amplifies the signal charge accumulated at this photo detector, the transfer element which transmits the signal charge accumulated at the aforementioned photo detector to the control electrode of the aforementioned amplifier, and the reset element which resets the charge of the control electrode of the aforementioned amplifier are provided. The control electrode of the transfer element of the pixel of each line is connected to the line line which corresponds in common, the line line of each line is connected to the correspondence circuit stage of the aforementioned vertical-scanning circuit, and the control electrode of the reset element of all pixels is connected to a reset control signal input terminal in common. And all transfer elements are set to ON through each aforementioned line line by setting the output of two or more circuit stages of the shift register of the aforementioned vertical-scanning circuit as the aforementioned predetermined logic state. And while setting the reset element of all pixels to ON and resetting the charge of a photo detector through a transfer element and a reset element by adding the aforementioned reset control signal to the reset element of all pixels By impressing the voltage which makes this amplifier a cut-off state through the reset element which was turned on on the occasion of this reset at the control electrode of an amplifier, the rushes current at the time of reset is reduced.

[0025] It can set to the solid state camera concerning such composition, and all the transfer elements of each line line can be set to ON by making the output of two or more circuit stages of the shift register of the aforementioned vertical-scanning circuit into a predetermined logic state at the time of reset, and the reset element of all pixels can be set to ON, and the charge of a photo detector can be reset through a transfer element and a reset element. Moreover, if the voltage which makes this amplifier a cut-off state through the reset element which was turned on on the occasion of this reset at the control electrode of an amplifier is impressed, it is lost that rushes current flows to an amplifier at the time of reset, and even if it resets many pixels simultaneously, it will be lost that rushes current excessive as the whole solid state camera flows.

[0026] In **** of further others of this invention The current regulator circuit and the aforementioned pixel which were prepared for each [which connected in common the output terminal of two or more pixels which consist of an amplified type photo-electric-translation means to be arranged in the shape of two-dimensional, and to accumulate and amplify the signal charge according to the lightwave signal respectively in a line and the direction of a train, and each pixel arranged in the direction of a train] train line of every In the solid state camera which carries out a selection drive and which has level and perpendicular each scanning circuit Continuation connection of two or more circuit stages should be made, and the aforementioned vertical-scanning circuit should be constituted, and should be equipped

with the shift register which can be set as a predetermined logic state for the output of two or more aforementioned circuit stages almost simultaneous according to the input of a predetermined control signal. The aforementioned pixel respectively the signal charge according to the lightwave signal The photo detector to accumulate, the amplifier which amplifies the signal charge accumulated at this photo detector, the transfer element which transmits the signal charge accumulated at the aforementioned photo detector to the control electrode of the aforementioned amplifier, and the reset element which resets the charge of the control electrode of the aforementioned amplifier are provided. The control electrode of the transfer element of the pixel of each line is connected to the line line which corresponds in common, the line line of each line is connected to the correspondence circuit stage of the aforementioned vertical-scanning circuit, and the control electrode of the reset element of all pixels is connected to a reset control signal input terminal in common. Moreover, it has a means to impress bias voltage to an amplifier through each train line in order that each train line may change into a cut-off state the amplifier of the pixel connected to each train line. And all transfer elements are set to ON through each aforementioned line line by setting the output of two or more circuit stages of the shift register of the aforementioned vertical-scanning circuit as the aforementioned predetermined logic state. And while setting the reset element of all pixels to ON and resetting the charge of a photo detector through a transfer element and a reset element by adding the aforementioned reset control signal to the reset element of all pixels By making the amplifier of all pixels into a cut-off state by the aforementioned bias voltage impression means in the case of this reset, the rushes current at the time of reset is reduced.

[0027] The charge of a photo detector can be emitted through a transfer element and a reset element by setting all transfer elements to ON through each line line, and setting the reset element of all pixels to ON with the aforementioned reset control signal by setting the output of two or more circuit stages of the shift register of a vertical-scanning circuit as a predetermined logic state also in this case. And the rushes current at the time of reset can be reduced by making the amplifier of all pixels into a cut-off state by the aforementioned bias voltage impression means in the case of this reset. Since the aforementioned bias voltage impression means can impress desired suitable bias voltage to the amplifier of a pixel independently with other elements, it can increase the flexibility of a design of each element of a pixel. That is, through the aforementioned transfer element and a reset element, the voltage by which a photo detector is depletion-ized completely can be supplied, and, on the other hand, the bias voltage which fully makes this amplifier a cut-off state can be independently impressed to the aforementioned amplifier, and it can design so that it may have the optimal property of respectively a request of a photo detector and an amplifier.

[0028]

[Embodiments of the Invention] Drawing 1 is the block diagram showing the composition of the outline of the solid state camera concerning this invention, and shows the example of two-dimensional image sensors. The solid state camera of this drawing is equipped with the pixel section 3 which has two or more pixels 1, the vertical-scanning circuit 5, the level read-out section 7, and the horizontal scanning circuit 9.

[0029] The pixel 1 equipped with a photodiode, an amplifier, etc. for light-receiving so that it might explain in detail later, respectively is arranged in the shape of a matrix, and the pixel section 3 is constituted. The vertical-scanning circuit 5 chooses the pixel for 1 level line (line line) of the pixel section 3 one by one, and consists of dynamic shift registers of the structure shown later. The level read-out section 7 accepts the charge of the pixel for 1 level line from the pixel section 3, and outputs this one by one based on the scanning pulse from the horizontal scanning circuit 9. The horizontal scanning circuit 9 is also constituted by the same dynamic shift register as the aforementioned perpendicular criminal-investigation circuit 5.

[0030] Signal phiSTV inputted into the vertical-scanning circuit 5 is a perpendicular start pulse, and serves as initial input data of a dynamic shift register. Moreover, perpendicular clock pulse phiCKV for shifting the dynamic shift register and perpendicular initialization pulse phiINTV are inputted into the vertical-scanning circuit 5.

[0031] Moreover, signal phiSTH inputted into the horizontal scanning circuit 9 is the start signal of the dynamic shift register which constitutes the horizontal scanning circuit 9, and phiCKH is a clock signal for a level shift. Moreover, level initialization pulse phiINTH for initializing the dynamic shift register which constitutes this horizontal scanning circuit 9 if needed is inputted into the horizontal scanning circuit 9.
[0032] In the solid state camera of drawing 1 , when used, for example for a still video camera etc., before pushing a shutter, a solid state camera carries out false operation, namely, although a scan is carried out, the output signal is taken as the state where it is not used. And if a shutter is pushed, initialization pulse phiINTV will be added to the vertical-scanning circuit 5 during a fixed period of about ten microseconds and start pulse phiSTV will be simultaneously made into H level, the whole page of the shift register of the vertical-scanning circuit 5 under false operation will be in a presetting state compulsorily, all pixels will be in a selection state, and the charge of all pixels can be reset.
[0033] Next, after make perpendicular start pulse phiSTV into L level, and making the vertical-scanning circuit 5 into a reset state, adding initialization pulse phiINTH also to the horizontal scanning circuit 9, and making level start pulse phiSTH into L level and changing the horizontal scanning circuit 9 into a reset state, it returns to normal operation and shift operation of each shift register is started. At this time, each pixel has started accumulation of image information, and if it returns to the usual operation and read-out operation is started after it makes L level again H level and perpendicular start pulse phiSTV and level start pulse phiSTH for initialization pulse phiINTV and phiINTH after progress of the predetermined exposure time and carries out forcible reset of each shift register, it can obtain the predetermined video signal by which time exposure was carried out.
[0034] In addition, in the solid state camera of drawing 1 , the usual read-out operation is in the state which made the low each initialization pulse phiINTV of the vertical-scanning circuit 5 and the horizontal scanning circuit 9, and phiINTH, respectively, shifts start signal phiSTV of a high level one by one by clock signal phiCKV in the vertical-scanning circuit 5, and chooses the pixel for 1 level line of the pixel section 3 one by one. The charge accumulated at the photodiode of each pixel for selected 1 level line is transmitted to the level read-out section 7. Next, by shifting start signal phiSTH of a high level one by one clock signal phiCKH by the horizontal scanning circuit 9, by this horizontal scanning circuit 9, the charge transmitted to the level read-out section 7 is horizontally transmitted one by one by 1 pixel, and it reads to the output terminal shell exterior.
[0035] Drawing 2 shows the detailed circuitry of the solid state camera of drawing 1 . The same portion as drawing 1 is shown by the same reference number in the solid state camera of drawing 2 . That is, it is constituted by the pixel section 3 which the solid state camera of drawing 2 also equipped with two or more pixels 1, the vertical-scanning circuit 5, the level read-out section 7, the horizontal scanning circuit 9, etc. In the circuit of drawing 2 , the pixel section 3 shall consist of pixels 1 of three line x3 train for simplification of explanation.
[0036] Each pixel 1 consists of reset switches QRST which consist of an MOS transistor for setting the switch QT for a transfer which consists of an MOS transistor for transmitting the charge of Amplifier QA and Photodiode PD which consists of a photodiode PD which is a photo detector, and a junction field effect transistor (JFET) to the gate of Amplifier QA, and the gate electrode of Amplifier QA as predetermined voltage. In addition, in a drawing, although the subscript is made each element, when expressing on behalf of the element of the same kind for simplification of explanation, a subscript may be omitted. In each pixel 1 shown in drawing 2 , the gate of the photodiode PD which is a light-receiving means, and Amplifier QA is separated on structure.
[0037] The source of the amplifier QA of the pixel perpendicularly arranged among the amplifiers QA of each pixel 1 is connected to the constant current source CSV of each train through the train line LV of each train (LV1-LV3). Each constant current source CSV serves as a load when operating Amplifier QA as a source follower. The other end of each constant current source CSV is connected to the predetermined power supply VEE in common.
[0038] The cathode of the photodiode PD of each pixel 1 is connected to the predetermined power supply VDD in common, and the anode is connected to the source of the switch QT for a transfer. The

drain of the switch QT for a transfer is connected to the gate of Amplifier QA, and the source of a reset switch QRST. The source of each amplifier QA is connected to each train line LV (LV1-LV3) in common for every train. The gate of each switch QT for a transfer is constituted so that it may connect with the vertical-scanning circuit 5 in common for every line and 1st vertical-scanning signal phiTR may be received. Vertical-scanning signal phiTR1 of each line - phiTR3 are connected to the output of each circuit stage of the vertical-scanning circuit 5. The gate of a reset switch QRST is connected to control signal phiPG [all / pixel], and the drain is constituted so that it may connect with the vertical-scanning circuit 5 in common horizontally and 2nd vertical-scanning signal phiRD may be supplied for every line. The drain of each amplifier QA is connected to the power supply VDD same in common as the anode of the aforementioned photodiode PD.

[0039] In addition, since the output of each circuit stage of the vertical-scanning circuit 5 supplies the 1st of a voltage level, and 2nd vertical-scanning signal phiTR(s) different, respectively and phiRDs different, respectively, it can also connect and constitute a predetermined voltage shift circuit in the output of each circuit stage of a shift register, respectively.

[0040] The level read-out section 7 is read for every train, and consists of a gate transistor QTC, capacity CT, and a switching device QH for level read-out. The upper limit of each train line LV is connected to the drain of the read-out gate transistor QTC, and the source of this read-out gate transistor QTC is connected to the drain of the switching device QH for level read-out of each train, and capacity CT. The other end of capacity CT is grounded. The gate of all the read-out gate transistors QTC is constituted so that it may connect in common and transfer pulse phiT can be supplied. Moreover, the gate of the switching device QH for level read-out is connected to the output of each circuit stage of the shift register of the horizontal scanning circuit 9 for every train. Furthermore, the source of the switching device QH for level read-out is connected to the video outlet terminal through the level output line HOUT in common.

[0041] In the solid state camera which has the above composition, reset of a pixel is performed as follows. That is, both initialization pulse phiINTV of the vertical-scanning circuit 5 and start pulse phiSTV are made into highness, and all the circuit stages of the vertical-scanning circuit 5 are preset, and it considers as the selection state of all pixels. By this, all (phiTR1 - phiTR3) of 1st vertical-scanning signal phiTR of all circuit stages are simultaneously made into highness, and the switch QT for a transfer of all pixels is set to ON. Moreover, reset control signal phiPG common to all pixels is added, and the reset switch QRST of all pixels is turned ON.

[0042] Let voltage of 2nd vertical-scanning signal phiRD (phiRD1 - phiRD3) be the voltage VGL which JFET which constitutes the amplifier QA of each pixel cuts off at this time.

[0043] thus, when it carries out, the residual charge accumulated at the photodiode PD of each pixel is discharged through the transfer element QT and the reset element QRST, and Photodiode PD is perfect -- a depletion -- it is-izing and reset And since the gate voltage of Amplifier QA is VGL as mentioned above, therefore this amplifier QA has cut off in this case, current does not flow to this amplifier QA. That is, the current with which the current which flows to Photodiode PD was amplified and amplified by Amplifier QA does not flow. For this reason, the rushes current of each pixel becomes very small, and it is lost that rushes current excessive as the whole solid state camera flows.

[0044] In addition, when reading a signal in the solid state camera of drawing 2 , while making initialization pulse phiINTV of the vertical-scanning circuit 5 into a low level and making start pulse phiSTV into highness, clock signal phiCKV is added and shift operation of the vertical-scanning circuit 5 is made to perform. By this, the pixel of each line is chosen one by one, and the signal accumulated at the selected pixel is outputted to the perpendicular read-out line LV. And it connected with each train line, and reads, the gate transistor QTC is set to ON by transfer pulse phiT, and the read-out charge of a signal is charged at the capacity CT of each train. Moreover, shift operation is made to perform also in the horizontal scanning circuit 9 by making low-level and start pulse phiSTH high-level for initialization pulse phiINTH, and adding clock signal phiCKH. The switching device QH for level read-out of each train is set to ON one by one, and the read-out signal of each train is supplied to the level output line HOUT by this, and is outputted to the video outlet terminal shell exterior.

[0045] Moreover, in reading such a signal, it turns ON the reset element QRST of all pixels by reset control signal phiPG. And to the selected line, voltage of 2nd vertical-scanning signal phiRD is made into the voltage VGH which the amplifier QA of each pixel is turned on [it] and activates, and let it be the aforementioned voltage VGL which Amplifier QA cuts off to a non-choosing pixel. In this state, even if it turns OFF the aforementioned control signal phiPG, the gate voltage of this amplifier QA is held by the gate stray capacity of Amplifier QA at the same value. Therefore, after turning OFF the reset element QRST of all pixels by reset control signal phiPG, the transfer element of the pixel of the line chosen by 1st vertical-scanning signal phiTR is turned ON. The signal charge accumulated at Photodiode PD is transmitted to the gate of Amplifier QA by this, and the gate voltage of this amplifier QA changes with it corresponding to a signal. Amplifier QA is operated as a source follower, this voltage is outputted to the train line LV, the horizontal scanning circuit 9 is scanned as mentioned above, and it reads outside one by one.

[0046] Drawing 3 shows the composition of an usable dynamic shift register to the horizontal scanning circuit and vertical-scanning circuit of a solid state camera concerning this invention. The dynamic shift register of drawing 3 is created using a CMOS process, and shows the example which used the so-called clocked inverter activated one by one by the clock pulse.

[0047] In the dynamic shift register of drawing 3 , two PMOS transistors P1 and P2 and two NMOS transistors N2 and N1 by which the series connection was carried out, for example between the positive supply voltage VDD and the negative supply voltage VSS constitute one step of clocked inverter. The PMOS transistors P3 and P4 and the NMOS transistors N4 and N3 constitute the 2nd step of clocked inverter, PMOS transistor P5, and P6 and two NMOS transistors N6 and N5 constitute the 3rd step of clocked inverter, two PMOS transistors P7 and P8 and two NMOS transistors N8 and N7 constitute the 4th step of clocked inverter, and it is the same as that of the following.

[0048] P2, N2, and the 2nd step constitute P8, N8, and the ********** CMOS inverter from P6, N6, and the 4th step from the PMOS transistor located in the center in the clocked inverter of each circuit stage, and the NMOS transistor, for example, the 1st step, in P4, N4, and the 3rd step. The transistor connected between each CMOS inverter and power supplies VDD and VSS is a transistor for control for activating these CMOS inverters.

[0049] The PMOS transistor P1, P5, and the gate of -- are connected to the internal clock signal line CP 1 among these transistors for control, and the PMOS transistors P3 and P7 and the gate of -- are connected to the internal clock signal line CP 2. Moreover, the transistor N1 and N5 for control of other electric conduction type, i.e., NMOS transistors, and the gate of -- are connected to the internal clock signal line CN1, and it connects with the NMOS transistors N3 and N7 and the internal clock signal line CN2 of others [gate] of --.

[0050] Moreover, start pulse phiST is supplied to the gate of each transistors P2 and N2 which constitute the 1st step of CMOS inverter. The 1st step of output of a CMOS inverter is connected to the gate of the 2nd step of input P4 of a CMOS inverter, i.e., a transistor, and a transistor N4, the 2nd step of output of a CMOS inverter is connected to the 3rd step of output of a CMOS inverter, and the 3rd step of output of a CMOS inverter is connected to the 4th step of input of a CMOS inverter one by one.

[0051] The dynamic shift register of drawing 3 was further equipped with the inverter INV2 and the OR gates OR1 and OR2 which constitute a simultaneous activation circuit, and is equipped with two more inverters INV3 and INV4. Initialization pulse phiINT is supplied to one [each] input of the OR gates OR1 and OR2. As for the input of another side of OR-gate OR1, clock pulse phicreatine kinase is supplied, and the signal with which the input of another side of other OR-gate OR2 reversed clock pulse phicreatine kinase by the inverter INV2 is supplied. It connects with the aforementioned internal clock signal line CN2, and the output of OR-gate OR1 is connected to the internal clock signal line CP 2 through the inverter INV4. It connects with the internal clock signal line CN1, and the output of OR-gate OR2 is connected to the internal clock signal line CP 1 through the inverter INV3.

[0052] In the dynamic shift register which has the above composition, when initialization pulse phiINT is low (L) level, clock pulse phicreatine kinase occurs in the output of OR-gate OR1, and the clock pulse which reversed clock pulse phicreatine kinase is supplied to the output of OR-gate OR2. Therefore,

when clock pulse phicreatine kinase is high (H) level, H level and the internal clock signal line CP 2 serve as [the internal clock signal line CN2] L level, and transistors P3 and P7, -- and N3 and N7, and -- are turned on. On the other hand, when clock signal phicreatine kinase is L level, the output of OR-gate OR2 serves as H level, and a transistor P1, P5, -- and N1 and N5, and -- are turned on. Therefore, the 1st inverter and 2nd inverter of each circuit stage are activated by turns by clock signal phicreatine kinase, and start pulse phiST is shifted one by one to the consecutive circuit stage.

[0053] on the other hand -- if initialization pulse phiINT is made into H level -- the level of clock pulse phicreatine kinase -- both the outputs of the OR gates OR1 and OR2 serve as H level irrespective of how Therefore, both the internal clock signal lines CN1 and CN2 serve as H level, and both the internal clock signal lines CP1 and CP2 serve as L level. For this reason, the transistors P1 and P3 for control of all clocked inverters, P5, P7, -- and N1, N3, N5 and N7, and -- are turned on simultaneously. That is, all clocked inverters are activated simultaneously.

[0054] Regardless of clock pulse phicreatine kinase, it is reversed by each inverter, and input signal phiST is high-speed and is transmitted to a latter circuit by this. Therefore, if start pulse phiST is made into L level, all also of the outputs S1 and S2 of all circuit stages and -- will be set to L level, and the outputs S1 and S2 of H level, then all circuit stages and -- will be set to H level in start pulse phiST. That is, the output to all circuit stages or the desired circuit stage can be set or preset almost in instant. Moreover, since all circuits are in an active state, it is stabilized and they can also continue reset or a presetting state for a long time. In addition, the time delay of the clocked inverter used for the usual solid state camera is usually several or less nanoseconds, though it has 1000 steps of clocked inverters, transfer of data is possible for it from an input stage to the last stage at below several micro second, and it can perform reset or presetting of each circuit stage mostly in an instant.

[0055] Drawing 4 shows other examples of composition of the dynamic shift register which can be used for the solid state camera of this invention. The dynamic shift register of drawing 4 is equipped with two CMOS inverters for every circuit stage. That is, the 1st circuit stage has the 1st CMOS inverter which consists of a PMOS transistor P11 and an NMOS transistor N11, and the 2nd CMOS inverter which consists of a PMOS transistor P12 and an NMOS transistor N12. The 2nd circuit stage is equipped with the 1st CMOS inverter which consists of a PMOS transistor P13 and an NMOS transistor N13, and the 2nd CMOS inverter which consists of a PMOS transistor P14 and an NMOS transistor N14, and is the same as that of the following. Cascade connection of each inverter is carried out one by one through the transfer gate. Namely, the output of an inverter which consists of transistors P11 and N11 is connected to the input of an inverter which consists of transistors P12 and N12 through the 1st transfer gate T1. The output of an inverter which consists of transistors P12 and N12 is connected to the input of an inverter which consists of transistors P13 and N13 through the 2nd transfer gate T2. It connects with the input of an inverter which consists of transistors P14 and N14 through the 3rd transfer gate T3, and the output of an inverter which consists of transistors P13 and N13 is the same as that of the following.

[0056] The transfer gates T1 and T3 and the gate by the side of the PMOS transistor of -- are connected to the internal clock signal line CP 1, and the gate of an NMOS transistor is connected to the internal clock signal line CN1. Moreover, the transfer gates T2 and T4 and the gate of the PMOS transistor of -- are connected to the internal clock line CP 2, and the gate of an NMOS transistor is connected to the internal clock signal line CN2.

[0057] The dynamic shift register of drawing 4 is equipped with the simultaneous activation circuit which consists of an inverter INV2 and the OR gates OR1 and OR2 like the thing of drawing 3 , and is equipped with the inverters INV4 and INV3 which reverse the output of the OR gates OR1 and OR2, respectively, and are supplied to the internal clock signal lines CP2 and CP1. The output of the OR gates OR1 and OR2 is connected to the internal clock signal lines CN2 and CN1 again.

[0058] In the dynamic shift register of drawing 4 , when initialization pulse phiINT is L level, the reversal clock pulse to which the output of the OR gates OR1 and OR2 reversed clock pulse phicreatine kinase and this clock pulse phicreatine kinase, respectively is outputted. These clock pulse phicreatine kinases and the reversal clock pulse of those are supplied to the internal clock signal lines CN2 and CN1, respectively. Moreover, inverters INV4 and INV3 are further reversed, respectively, and clock

pulse phicreatine kinase outputted from the OR gates OR1 and OR2, respectively and its reversal clock pulse are supplied to the internal clock signal lines CP2 and CP1, respectively. That is, clock pulse phicreatine kinase is supplied for the clock pulse which reversed clock signal phicreatine kinase to the internal clock signal line CP 2 to the internal clock signal line CP 1.
[0059] Therefore, when clock pulse phicreatine kinase is H level, the transfer gates T2 and T4 and -- flow, and when clock pulse phicreatine kinase is L level, the transfer gates T1 and T3 and -- flow. That is, a flow and un-flowing the transfer gates T1, T2, T3, and T4 and -- are presupposed by turns by clock signal phicreatine kinase. It is transmitted to the circuit stage of one by one consecutiveness [like / common knowledge] of start pulse phiST by this, and shift operation is performed.
[0060] On the other hand, when initialization pulse phiINT is H level, both the outputs of the OR gates OR1 and OR2 serve as H level irrespective of the level of clock pulse phicreatine kinase. For this reason, the internal clock signal lines CN1 and CN2 serve as L level, and all the transfer gates T1, T2, T3, and T4 and -- flow through both the H level and internal clock signal lines CP1 and CP2 of both. That is, direct cascade connection of the inverter of all circuit stages will be carried out. Therefore, while start pulse phiST is reversed one by one, it is directly transmitted by each inverter. Therefore, it becomes possible to also set in the circuit of drawing 4 , and to reset or preset each circuit stage in an instant.
[0061] In addition, in above-mentioned explanation, although explained per two kinds of things as a dynamic shift register, it is clear to this invention that the dynamic shift register of various form can be used. That is, each circuit stage consists of 1 set of two-step dynamic form inverter circuits, and at the time of an active state, if another side is a dynamic shift register of form which transmits an input signal to the circuit stage of one by one consecutiveness as an inactive state substantially, this invention is substantially [one of the two] applicable. 1 set of two-step dynamic form inverters can be simultaneously activated in these cases, an input signal can be transmitted to the circuit stage of direct consecutiveness over two or more circuit stage, and reset and presetting can be made to perform compulsorily in an instant.
[0062] Next, drawing 5 shows the circuitry of the solid state camera concerning another ******** of this invention. Also in drawing 5 , the same portion as aforementioned drawing 1 is shown by the same reference number. Moreover, in the solid state camera of drawing 5 , each train lines LV1, LV2, and LV3 in the solid state camera of aforementioned drawing 2 are connected to the predetermined bias voltage VPU through the switching devices QPU1, QPU2, and QPU3 which consist of MOS transistors for pull-up etc., respectively. The gate of each switching devices QPU1, QPU2, and QPU3 is constituted so that it may connect in common and predetermined control signal phiPU can be supplied. Moreover, even if the gate of Amplifier QA is the read-out voltage VGH of Amplifier QA, let bias voltage VPU be the voltage which this amplifier QA cuts off. Other portions are the same as the circuit of drawing 2 , and the same reference number and the same reference mark are given to the same portion.
[0063] In resetting a pixel in the solid state camera of drawing 5 , like the case of drawing 2 , the whole page of the vertical-scanning circuit 5 is preset, the 1st vertical-scanning circuit phiTR1-TR3 is added to the switch QT for a transfer of all pixels, and it sets this switch QT for a transfer to ON. Moreover, control signal phiPG is added and the reset switch QRST of all pixels is turned ON. Let voltage of 2nd vertical-scanning signal phiRD1 - phiRD3 be the read-out voltage VGH of the amplifier QA of each pixel section at this time.
[0064] Furthermore, bias of each train lines LV1-LV3 is carried out to the aforementioned bias voltage VPU by control signal phiPU by setting the switching device QPU for pull-up of each train to ON at this time. As mentioned above, the gate of Amplifier QA reads this bias voltage VPU, and even if it is voltage VGH, it is taken as the voltage which Amplifier QA cuts off. By this, where Amplifier QA is cut off, the residual charge of Photodiode PD is emitted through the transfer element QT and the reset element QRST, and reset of a pixel is performed. And Photodiode PD is reset in this case by the state where the reverse bias was carried out to the read-out voltage VGH of Amplifier QA. However, by the switching device QPU for pull-up, the source voltage of each amplifier QA is the aforementioned bias voltage VPU, and current does not flow to Amplifier QA. That is, the excessive rushes current at the time of reset can be prevented. In addition, when reading a signal, where the switching device QPU for

pull-up is considered as a cut-off, it carries out like the case of the solid state camera of aforementioned drawing 2 .

[0065] In the solid state camera of above-mentioned drawing 2 and drawing 5 , it is desirable to constitute as a property of the photo detector of each pixel, so that a perfect depletion may be formed at the time of reset.

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TECHNICAL FIELD

[The technical field to which invention belongs] Concerning a solid state camera, this invention is used for an electronic still camera etc., and instant-reset of all pixels is possible for it, and it relates to the solid state camera which can moreover reduce the rushes current at the time of reset sharply.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] Drawing 6 shows the composition of the outline of the conventional solid state camera, and shows the example of two-dimensional image sensors. The equipment of this drawing is considered as the pixel composition of three line x3 train for simplification of explanation. Moreover, although the subscript is given to the reference mark of each element in the drawing, a subscript may be omitted when expressing on behalf of the element of the same kind for simplification of explanation.
[0003] With the equipment of drawing 6 , the static induction transistor (SIT) is used as an example of an amplified type photo detector as each pixel. That is, the static inductions transistor QS11, QS12, QS13, QS21, QS22, QS23, QS31, QS32, and QS33 which constitute each pixel are arranged in the shape of [of three line x3 train] a matrix.
[0004] Moreover, the vertical-scanning circuit VSR for choosing the pixel of each train one by one for every line is formed. That is, the gate of the static induction transistor arranged among the pixels arranged in the shape of a matrix at each line writing direction is connected to each circuit stage of the shift register of the vertical-scanning circuit VSR through each line line GV1, GV2, and GV3 in common. For example, the gate of static inductions transistor QS11, QS12, and QS13 is connected to the vertical-scanning circuit VSR through both the line lines GV1, and the gate of each static inductions transistor QS21, QS22, and QS23 is connected to the vertical-scanning circuit VSR through the line line GV2. All circuit stages are reset or preset by impression of initialization signal phiINTV, and the vertical-scanning circuit VSR can change all the line lines GV1, GV2, and GV3 into the selection state by it.
[0005] Moreover, the source of the static induction transistor of the pixel of each train is connected common to the train lines LV1, LV2, and LV3 of the train, and each train line is connected to the predetermined power supply VEE through the constant current source CSV. Each constant current source CSV serves as a load of the static induction transistor QS of each pixel at the time of signal read-out from each pixel. The drain of the static induction transistor QS of each pixel is connected to the predetermined power supply VDD in common. The end of each train lines LV1, LV2, and LV3 is grounded through the transistors QRSTV1, QRSTV2, and QRSTV3 for perpendicular reset for resetting each train line. Reset-signal phiRSTV for perpendicular read-out lines explained later is supplied to each transistor for perpendicular reset.
[0006] The other end of each train lines LV1, LV2, and LV3 is connected to the drain of each transistor QH1, QH2, and QH3 for a level output through each switch QT1, QT2, and QT3 for a transfer. The source of each transistor for a level output is connected to the common level output line HOUT, and this level output line HOUT is connected to the video outlet terminal for supplying an image pck-up signal outside. Moreover, the source of each transistors QT1, QT2, and QT3 for a transfer is grounded through each capacity CT1, CT2, and CT3.
[0007] The gate of the transistors QT1, QT2, and QT3 for a transfer of each train is connected in common, and transfer pulse phiT is supplied. Moreover, the gate of the level read-out transistors QH1-QH3 is connected to each circuit stage of the horizontal scanning circuit HSR. Like [the horizontal scanning circuit HSR] the aforementioned vertical-scanning circuit VSR, it has a shift register and, as

for this shift register, the thing in which the set or reset of all circuit stages is possible is used by level initialization signal phiINTH.

[0008] When used for example, for an electronic still camera, the solid state camera of drawing 6 operates by adding perpendicular start signal phiSTV to the vertical-scanning circuit VSR, and adding clock signal phiCKV for a perpendicular shift after progress of the predetermined exposure time, so that the shift register of the vertical-scanning circuit VSR may shift the aforementioned start signal phiSTV to each circuit stage one by one. Each line lines GV1, GV2, and GV3 are chosen one by one by this. The signal charge according to the incident light is accumulated at each static induction transistor QS, and the voltage corresponding to the charge by which this static induction transistor operated as a source follower, and was accumulated is outputted to each train line LV by applying predetermined selection voltage to the gate voltage in the selected line. That is, the signal from the static induction transistor QS of the selected line is simultaneously outputted to each perpendicular read-out line LV.

[0009] And after making it flow through the transfer transistor QT of each train by transfer signal phiT at this time and charging a signal charge at capacity CT1, CT2, and CT3, QT is intercepted, and the signal for every train is outputted to the level output line HOUT by setting the level read-out transistor QH to ON one by one by the vertical-scanning circuit HSR.

[0010] By the way, when such a solid state camera is used for example, for an electronic still camera, after resetting all pixels at the moment of pushing a shutter, the image pck-up of a photographic subject picture is performed. In the solid state camera of drawing 6 , reset of all pixels is performed as follows.

[0011] That is, the vertical-scanning circuit VSR is controlled by initialization signal phiINTV, clock signal phiCKV, and scanning start signal phiSTV including a shift register. If initialization signal phiINTV and phiSTV are made into highness, all the circuit stages of the vertical-scanning circuit VSR are preset, all the line lines GV1, GV2, and GV3 become highness, and all pixels will be in a selection state. On the other hand, if initialization signal phiINTV is made into highness and scanning start signal phiSTV is made into a low, each circuit stage of the vertical-scanning circuit VSR is reset, and all pixels will be in the state where it does not choose. If initialization signal phiINTV is made into a low, the vertical-scanning circuit VSR will start the usual shift operation, whenever clock signal phiCKV enters from the time of start signal phiSTV becoming highness, each line lines GV1, GV2, and GV3 serve as a high level one by one, and the pixel of one line is chosen at a time one by one.

[0012] And in order to reset all pixels in the solid state camera of drawing 6 , reset-signal phiRSTV only for perpendicular read-out is first made into highness, the transistors 1-QRSTV 3 for perpendicular reset of each train are set to ON, and each train lines LV1, LV2, and LV3 are connected to a gland.

[0013] Next, both aforementioned initialization signal phiINTV of the vertical-scanning circuit VSR and scanning start signal phiSTV are made into highness, and each circuit stage of the vertical-scanning circuit VSR is changed into a presetting state. By this, each line lines GV1, GV2, and GV3 of both become high-level, and will be in the selection state of all pixels. The high-level voltage of each line lines GV1, GV2, and GV3 in this case, i.e., the voltage of control signal phiSRs 1-3, is set up so that it may become the voltage VRSTP for reset of static inductions transistor 11-QS 33.

[0014] As everyone knows, an inversion layer is formed in the gate electrode lower part of each static inductions transistor QS11-QS33, a channel is made between the source drains of these static inductions transistor 11-QS 33, the residual charge charged at the gate flows out, and reset of all pixels is performed by this. At this time, the current by the outflow of the residual charge by reset flows simultaneously to the static inductions transistor QS11-QS33 of each pixel.

[Translation done.]

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MEANS

[Means for Solving the Problem] In the solid state camera possessing the scanning circuit for according to the 1st **** of this invention, choosing two or more pixels which perform photo electric translation, and two or more aforementioned pixels one by one, and reading them, in order to attain the above-mentioned purpose Continuation connection of two or more circuit stages should be made, and the aforementioned scanning circuit should be constituted, and should be equipped with the shift register which can be set as a predetermined logic state for the output of two or more aforementioned circuit stages almost simultaneous according to the input of a predetermined control signal. The photo detector to which the aforementioned pixel accumulates the signal charge according to the lightwave signal at least respectively, While choosing two or more pixels by having had the amplifier which amplifies the signal charge accumulated at this photo detector, and setting the output of two or more circuit stages of the shift register of the aforementioned scanning circuit as the aforementioned predetermined logic state The rushes current at the time of reset is reduced by resetting the charge of the aforementioned photo detector, where the aforementioned amplifier is cut off in two or more selected pixels.
[0019] With such composition, where the aforementioned amplifier is cut off in two or more pixels which chose and chose two or more pixels with the shift register of the aforementioned scanning circuit, the charge of the aforementioned photo detector is reset. Therefore, it is lost that rushes current flows to an amplifier at the time of reset, and it is lost that excessive rushes current flows though all the pixels in the solid state camera which has many pixels are reset simultaneously. Therefore, it becomes without the reliability of a solid state camera not falling and moreover the voltage of each portion in the chip of a solid state camera causing a big change by rushes current, and a solid state camera can demonstrate an original performance now exactly.
[0020] in this case, the pixel of each above shall possess the transfer element which transmits further the signal charge accumulated at the aforementioned photo detector to the control electrode of the aforementioned amplifier, and the reset element which resets the charge of the control electrode of the aforementioned amplifier, and shall reset the charge of a photo detector by setting both the aforementioned transfer element and the aforementioned reset element to ON
[0021] By taking such pixel composition, it becomes possible to emit the charge accumulated at the photo detector through the aforementioned transfer element and a reset element, where an amplifier is cut off by applying the voltage which sets the aforementioned transfer element and a reset element to ON at both the times of reset, and cuts off this amplifier to the control electrode of an amplifier through a reset element.
[0022] Furthermore, in case the charge of a photo detector is reset by setting both the aforementioned transfer element and a reset element to ON, it can also constitute so that the bias voltage impression means for impressing bias voltage to the aforementioned amplifier and holding the aforementioned amplifier in the cut-off state may be included.
[0023] In this case, the bias voltage for changing the aforementioned amplifier into a cut-off state to the aforementioned amplifier at the time of reset of a pixel by the above-mentioned bias voltage impression means can be impressed. Therefore, the property of a photo detector and an amplifier can be set as the

independently optimal respectively thing, where an amplifier is cut off completely, perfect depletion-ization of a photo detector can be attained, the flexibility of a design of each element increases, and a quality solid state camera can be realized.

[0024] Moreover, two or more pixels which consist of an amplified type photo-electric-translation means to be arranged in the shape of two-dimensional, and to accumulate and amplify the signal charge according to the lightwave signal respectively in a line and the direction of a train in other **** of this invention, In the current regulator circuit prepared for each [which connected in common the output terminal of each pixel arranged in the direction of a train] train line of every, and the solid state camera which carries out the selection drive of the aforementioned pixel and which has level and perpendicular each scanning circuit Continuation connection of two or more circuit stages should be made, and the aforementioned vertical-scanning circuit should be constituted, and should be equipped with the shift register which can be set as a predetermined logic state for the output of two or more aforementioned circuit stages almost simultaneous according to the input of a predetermined control signal. The aforementioned pixel respectively the signal charge according to the lightwave signal The photo detector to accumulate, the amplifier which amplifies the signal charge accumulated at this photo detector, the transfer element which transmits the signal charge accumulated at the aforementioned photo detector to the control electrode of the aforementioned amplifier, and the reset element which resets the charge of the control electrode of the aforementioned amplifier are provided. The control electrode of the transfer element of the pixel of each line is connected to the line line which corresponds in common, the line line of each line is connected to the correspondence circuit stage of the aforementioned vertical-scanning circuit, and the control electrode of the reset element of all pixels is connected to a reset control signal input terminal in common. And all transfer elements are set to ON through each aforementioned line line by setting the output of two or more circuit stages of the shift register of the aforementioned vertical-scanning circuit as the aforementioned predetermined logic state. And while setting the reset element of all pixels to ON and resetting the charge of a photo detector through a transfer element and a reset element by adding the aforementioned reset control signal to the reset element of all pixels By impressing the voltage which makes this amplifier a cut-off state through the reset element which was turned on on the occasion of this reset at the control electrode of an amplifier, the rushes current at the time of reset is reduced.

[0025]

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, when resetting simultaneously the shell constituted so that a photo detector might be reset, where the amplifier of each pixel is cut off in a solid state camera, when resetting, and the solid-state-camera smell all pixel containing many pixels according to this invention, it can prevent that excessive rushes current occurs. Therefore, while being able to prevent the fall of the reliability of the solid state camera by rushes current, it enables a solid state camera for having a bad influence on a solid state camera to be prevented by the voltage variation of each part of the inside of a chip by rushes current, and to demonstrate an original performance by it. At the moment of turning off a shutter, all pixel simultaneous reset can use such a solid state camera for a required electronic still camera etc., and it can obtain a good result.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Thus, in the solid state camera which has the conventional amplified type image pck-up element, when all pixels were reset, it was resetting by making the pixel section including an amplification means into one by choosing all pixels simultaneously. For this reason, at the time of reset, all the amplification meanses in each pixel are also turned on [them] simultaneously, and the current of all amplification meanses flows all at once. Although the current at this time is called rushes current, since all pixels are it turned on that the rushes current of each pixel is small simultaneously, big rushes current flows with the whole image pck-up equipment.
[0016] For example, though the rushes current of each pixel is a number microampere, when the number of pixels is 1 million pixels, with the whole image pck-up equipment, it amounts to several A. When the current which reaches in the chip of a solid state camera at several A flowed, there was also a possibility of the fall of the reliability by electromigration becoming a problem, and the voltage of each [in a chip] portion having not fitted in the predetermined voltage range with the parasitism impedance of each portion in a chip, and the performance which the chip expected as a solid state camera not having been demonstrated, or producing the malfunction by rushes current etc.
[0017] Therefore, the purpose of this invention is to enable it to also prevent the fall of the reliability of a solid state camera exactly while the excessive rushes current at the time of reset is prevented in the solid state camera which used the amplified type pixel and the whole chip of a solid state camera enables it to demonstrate a predetermined performance in view of the trouble in such conventional equipment.

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EXAMPLE

[Example] In addition, in the solid state camera in above-mentioned drawing 2 and drawing 5 , the voltage of each power supply and a signal is specifically set up as follows, and a high result is obtained. That is, it is referred to as read-out voltage VGH=-1V which the amplifier QA of each aforementioned pixel is turned on [it], and activates on condition that supply voltage VDD=5V and VEE=0V. And the voltage VGL of 2nd vertical-scanning signal phiRD supplied to the drain of the reset element of each pixel at the time of the reset in the composition of aforementioned drawing 2 is good -3V. Moreover, the bias voltage VPU for cutting off each pixel in the composition of aforementioned drawing 5 carries out to the voltage (more than +1V [for example,]) which this amplifier QA cuts off, even if the gate voltage of Amplifier QA is VGH=-1V.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the composition of the outline of the solid state image pickup device concerning this invention.
[Drawing 2] It is the electrical diagram showing the detailed composition of the solid state camera concerning the 1st operation gestalt of this invention.
[Drawing 3] It is the electrical diagram showing the composition of an usable shift register in the scanning circuit of the solid state camera concerning this invention.
[Drawing 4] It is the electrical diagram showing other composition of an usable shift register in the scanning circuit of the solid state image pickup device concerning this invention.
[Drawing 5] It is the electrical diagram showing the detailed composition of the solid state image pickup device concerning the 2nd operation gestalt of this invention.
[Drawing 6] It is the electrical diagram showing the composition of the conventional solid state camera.
[Description of Notations]
1 Pixel
3 Pixel Section
5 Vertical-Scanning Circuit (VSR)
7 Level Read-out Section
9 Horizontal Scanning Circuit (HSR)
PD11, --, PD33 Photodiode
QT11, --, QT33 Transfer element
QA11, --, QA33 Amplifier
QRST11, --, QRST33 Reset element
CSV1, --, CSV3 Constant current source
QTC1, --, QTC3 Read-out gate transistor
CT1, --, CT3 Capacity for accumulation
QH1, --, QH3 Switching device for level read-out
QPU1, --, QPU3 Switching device for pull-up

[Translation done.]

* NOTICES *

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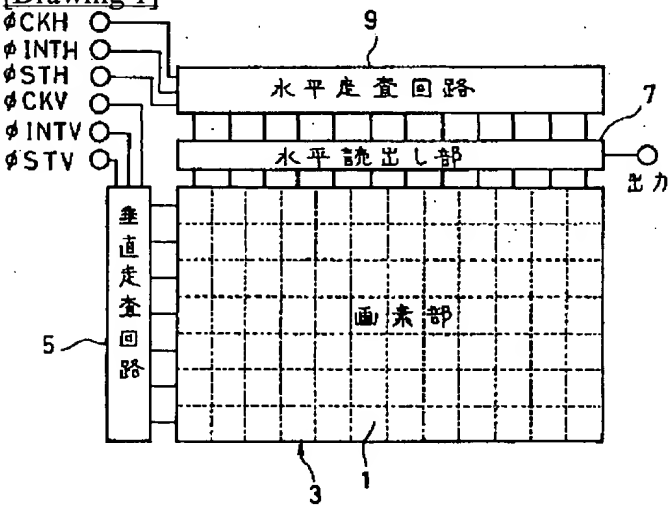
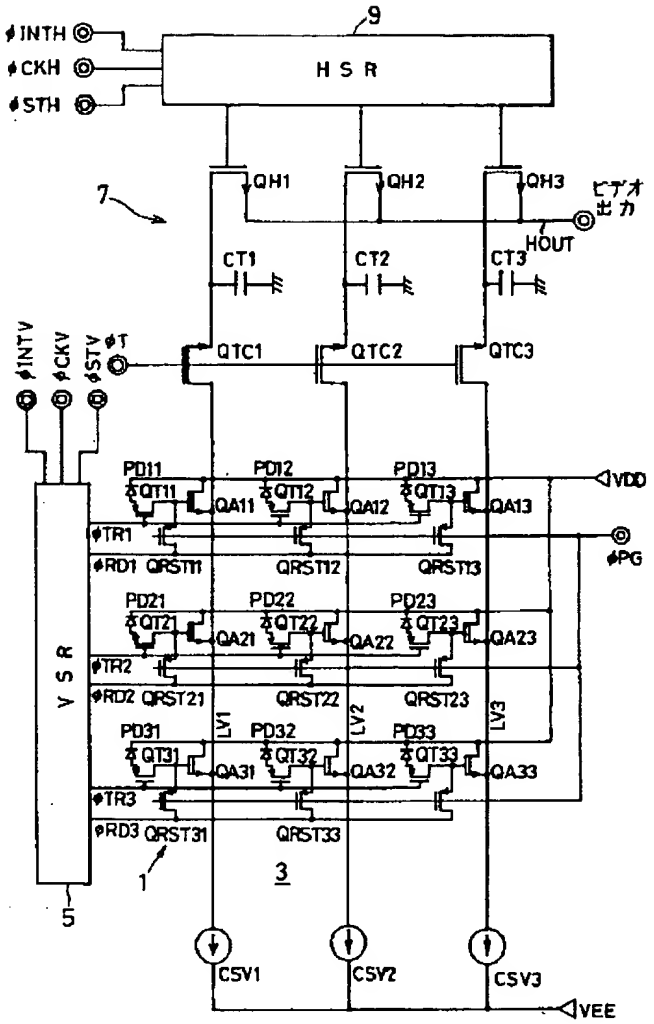
DRAWINGS

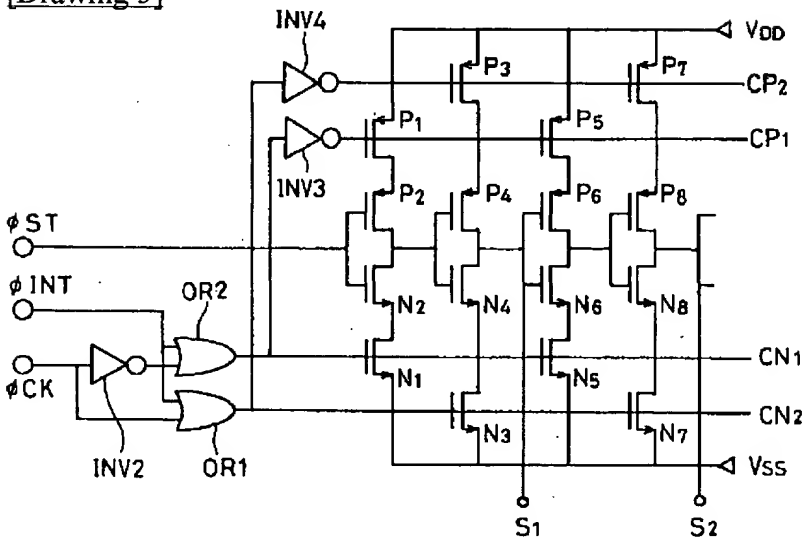
[Drawing 1]



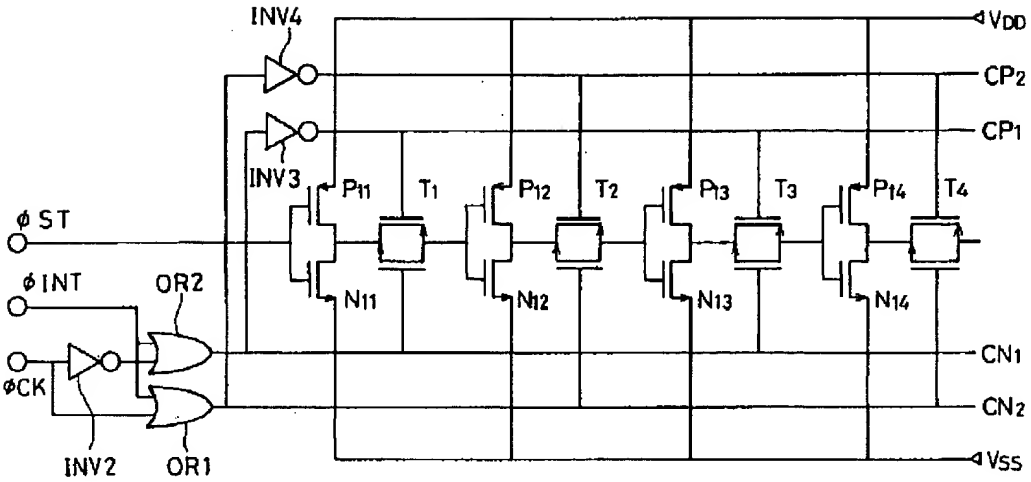
[Drawing 2]



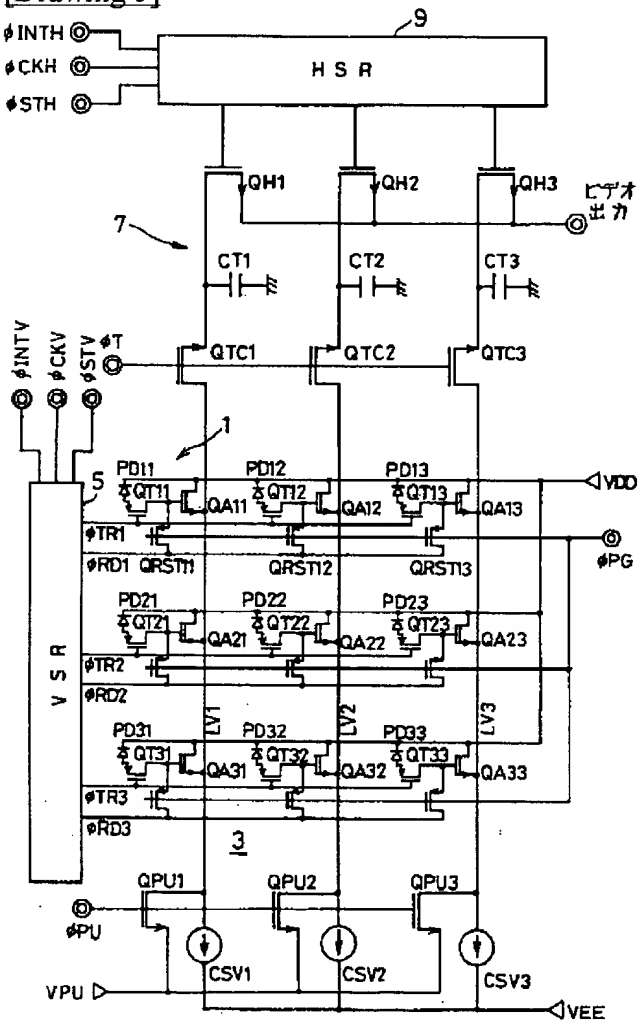
[Drawing 3]



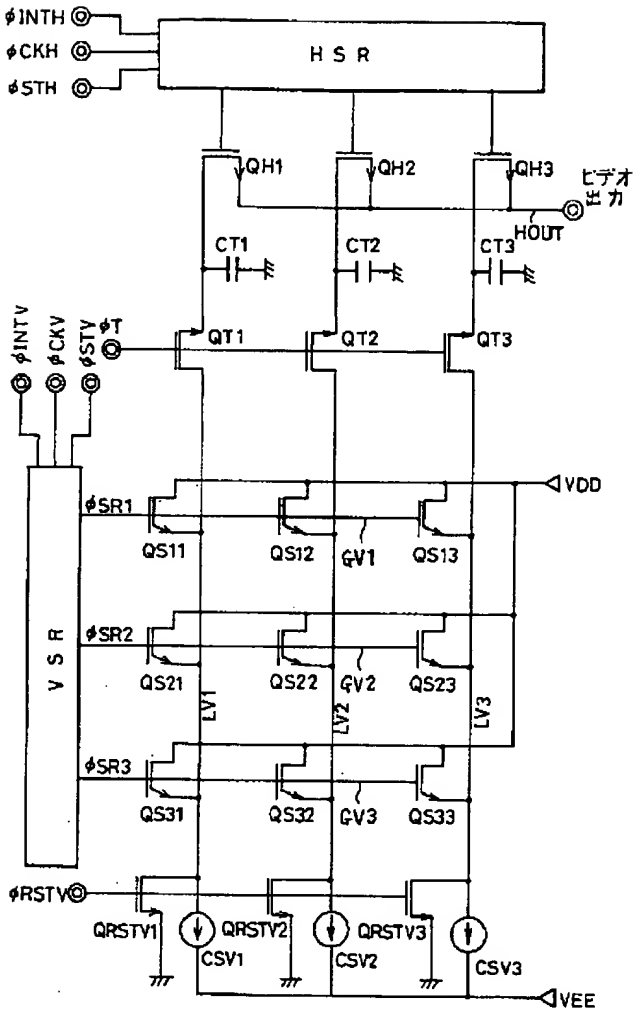
[Drawing 4]



[Drawing 5]



[Drawing 6]



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Ｈ０１Ｌ　27/146			Ｈ０１Ｌ　27/14	Ａ	

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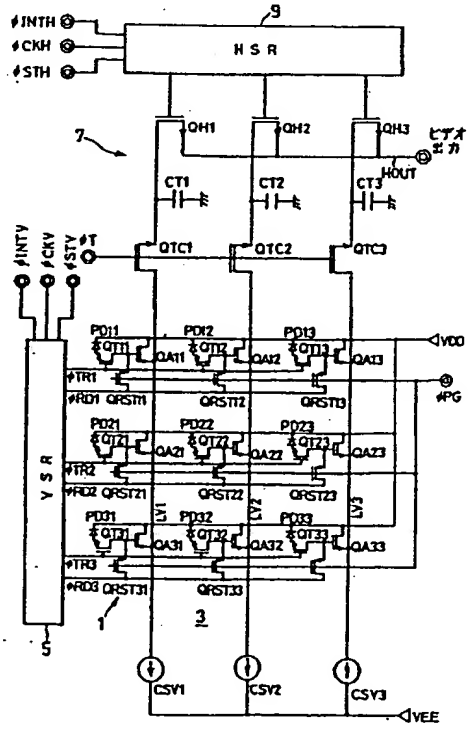
(54)【発明の名称】　固体撮像装置

(57)【要約】

【課題】　固体撮像装置の全画素をリセットする場合の過大なラッシュ電流を防止する。

【解決手段】　光電変換を行なう複数の画素１と、複数の画素１を順次選択する走査回路５，９を有する固体撮像装置において、走査回路として複数の回路段の出力をほぼ同時に所定の論理状態に設定可能なシフトレジスタを備えたものを使用し、画素１として受光素子ＰＤと該受光素子ＰＤに蓄積された信号電荷を増幅する増幅素子ＱＡを備えたものを使用する。走査回路５のシフトレジスタの複数の回路段の出力を前記所定の論理状態に設定して複数の画素１を選択し、選択した複数の画素１において増幅素子ＱＡをカットオフした状態で受光素子ＰＤの電荷をリセットする。



【特許請求の範囲】

【請求項１】　光電変換を行なう複数の画素と、前記複数の画素を順次選択して読み出すための走査回路を具備する固体撮像装置において、

前記走査回路は、複数の回路段が継続接続されて構成され所定の制御信号の入力に応じて前記複数の回路段の出力をほぼ同時に所定の論理状態に設定可能なシフトレジスタを備え、

前記画素は各々少なくとも光信号に応じた信号電荷を蓄積する受光素子と、該受光素子に蓄積された信号電荷を増幅する増幅素子とを備え、かつ前記走査回路のシフトレジスタの複数の回路段の出力を前記所定の論理状態に設定することによって複数の画素を選択するとともに、選択した複数の画素において前記増幅素子をカットオフした状態で前記受光素子の電荷をリセットすることによりリセット時のラッシュ電流を低減したことを特徴とする固体撮像装置。

【請求項２】　前記各々の画素は、さらに、前記受光素子に蓄積された信号電荷を前記増幅素子の制御電極に転送する転送素子と、前記増幅素子の制御電極の電荷をリセットするリセット素子とを具備し、前記転送素子および前記リセット素子を共にオンとして受光素子の電荷をリセットすることを特徴とする請求項１に記載の固体撮像装置。

【請求項３】　さらに、前記転送素子およびリセット素子を共にオンとして受光素子の電荷をリセットする際に、前記増幅素子にバイアス電圧を印加して前記増幅素子をカットオフ状態に保持するためのバイアス電圧印加手段を含むことを特徴とする請求項２に記載の固体撮像装置。

【請求項４】　行および列方向に２次元状に配置され各々光信号に応じた信号電荷を蓄積し増幅する増幅型光電変換手段からなる複数の画素と、列方向に配列された各画素の出力端子を共通に接続した各列ライン毎に設けられた定電流回路と、前記画素を選択駆動する水平及び垂直各走査回路とを有する固体撮像装置において、

前記垂直走査回路は複数の回路段が継続接続されて構成され所定の制御信号の入力に応じて前記複数の回路段の出力をほぼ同時に所定の論理状態に設定可能なシフトレジスタを備え、

前記画素は各々、光信号に応じた信号電荷を蓄積する受光素子と、該受光素子に蓄積された信号電荷を増幅する増幅素子と、前記受光素子に蓄積された信号電荷を前記増幅素子の制御電極に転送する転送素子と、前記増幅素子の制御電極の電荷をリセットするリセット素子とを具備し、各行の画素の転送素子の制御電極は共通に対応する行ラインに接続され、各行の行ラインは前記垂直走査回路の対応回路段に接続され、すべての画素のリセット素子の制御電極は共通にリセット制御信号入力端子に接続され、かつ前記垂直走査回路のシフトレジスタの複数の回路段の出力を前記所定の論理状態に設定することによって前記各行ラインを介してすべての転送素子をオンとし、かつ前記リセット制御信号をすべての画素のリセット素子に加えることによって全画素のリセット素子をオンとし、受光素子の電荷を転送素子およびリセット素子を介してリセットするとともに、このリセットの際にオンとなったリセット素子を介して増幅素子の制御電極に該増幅素子をカットオフ状態とする電圧を印加することにより、リセット時のラッシュ電流を低減したことを特徴とする固体撮像装置。

【請求項５】　行および列方向に２次元状に配置され各々光信号に応じた信号電荷を蓄積し増幅する増幅型光電変換手段からなる複数の画素と、列方向に配列された各画素の出力端子を共通に接続した各列ライン毎に設けられた定電流回路と、前記画素を選択駆動する水平及び垂直各走査回路とを有する固体撮像装置において、

前記垂直走査回路は複数の回路段が継続接続されて構成され所定の制御信号の入力に応じて前記複数の回路段の出力をほぼ同時に所定の論理状態に設定可能なシフトレジスタを備え、

前記画素は各々、光信号に応じた信号電荷を蓄積する受光素子と、該受光素子に蓄積された信号電荷を増幅する増幅素子と、前記受光素子に蓄積された信号電荷を前記増幅素子の制御電極に転送する転送素子と、前記増幅素子の制御電極の電荷をリセットするリセット素子とを具備し、各行の画素の転送素子の制御電極は共通に対応する行ラインに接続され、各行の行ラインは前記垂直走査回路の対応回路段に接続され、すべての画素のリセット素子の制御電極は共通にリセット制御信号入力端子に接続され、

各列ラインは、各列ラインに接続された画素の増幅素子をカットオフ状態にするために各列ラインを介して増幅素子にバイアス電圧を印加する手段を備え、かつ前記垂直走査回路のシフトレジスタの複数の回路段の出力を前記所定の論理状態に設定することによって前記各行ラインを介してすべての転送素子をオンとし、かつ前記リセット制御信号をすべての画素のリセット素子に加えることによって全画素のリセット素子をオンとし、受光素子の電荷を転送素子およびリセット素子を介してリセットするとともに、このリセットの際に前記バイアス電圧印加手段によって全画素の増幅素子をカットオフ状態とすることにより、リセット時のラッシュ電流を低減したことを特徴とする固体撮像装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、固体撮像装置に関し、例えば電子スチルカメラなどに使用され、全画素の瞬時的なリセットが可能でありしかもリセット時のラッシュ電流を大幅に低減することができる固体撮像装置に関する。

【0002】
【従来の技術】図6は、従来の固体撮像装置の概略の構成を示し、2次元のイメージセンサの例を示している。同図の装置は、説明の簡略化のため3行×3列の画素構成としている。また、図面では各素子の参照符号に添字が付されているが、説明の簡略化のため同じ種類の素子を代表して表現する場合には添字は省略することがある。
【0003】図6の装置では各画素としては、増幅型受光素子の例として静電誘導トランジスタ（ＳＩＴ）を使用している。すなわち、各画素を構成する静電誘導トランジスタＱＳ１１，ＱＳ１２，ＱＳ１３，ＱＳ２１，ＱＳ２２，ＱＳ２３，ＱＳ３１，ＱＳ３２，ＱＳ３３が3行×3列のマトリクス状に配置されている。
【0004】また、各列の画素を行ごとに順次選択するための垂直走査回路ＶＳＲが設けられている。すなわち、マトリクス状に配置された画素のうち各行方向に配置された静電誘導トランジスタのゲートが共通にそれぞれの行ラインＧＶ１，ＧＶ２，ＧＶ３を介して垂直走査回路ＶＳＲのシフトレジスタの各回路段に接続されている。例えば静電誘導トランジスタＱＳ１１，ＱＳ１２，ＱＳ１３のゲートは共に行ラインＧＶ１を介して垂直走査回路ＶＳＲに接続され、各静電誘導トランジスタＱＳ２１，ＱＳ２２，ＱＳ２３のゲートは行ラインＧＶ２を介して垂直走査回路ＶＳＲに接続されている。垂直走査回路ＶＳＲは、初期化信号φＩＮＴＶの印加によって全回路段がリセットまたはプリセットされて全ての行ラインＧＶ１，ＧＶ２，ＧＶ３を選択状態にすることができるのである。
【0005】また、各列の画素の静電誘導トランジスタのソースはその列の列ラインＬＶ１，ＬＶ２，ＬＶ３に共通に接続され、各列ラインは定電流源ＣＳＶを介して所定の電源ＶＥＥに接続されている。各定電流源ＣＳＶは各画素からの信号読み出し時に各画素の静電誘導トランジスタＱＳの負荷となるものである。各画素の静電誘導トランジスタＱＳのドレインは共通に所定の電源ＶＤＤに接続されている。各列ラインＬＶ１，ＬＶ２，ＬＶ３の一端はそれぞれの列ラインをリセットするための垂直リセット用トランジスタＱＲＳＴＶ１，ＱＲＳＴＶ２，ＱＲＳＴＶ３を介して接地されている。各々の垂直リセット用トランジスタには後に説明する垂直読み出し線用リセット信号φＲＳＴＶが供給されている。
【0006】各列ラインＬＶ１，ＬＶ２，ＬＶ３の他端はそれぞれの転送用スイッチＱＴ１，ＱＴ２，ＱＴ３を介してそれぞれの水平出力用トランジスタＱＨ１，ＱＨ２，ＱＨ３のドレインに接続されている。各水平出力用トランジスタのソースは共通の水平出力線ＨＯＵＴに接続され、該水平出力線ＨＯＵＴは撮像信号を外部に供給するためのビデオ出力端子に接続されている。また、各転送用トランジスタＱＴ１，ＱＴ２，ＱＴ３のソースはそれぞれの容量ＣＴ１，ＣＴ２，ＣＴ３を介して接地されている。
【0007】各列の転送用トランジスタＱＴ１，ＱＴ２，ＱＴ３のゲートは共通に接続され転送パルスφＴが供給される。また、水平読み出しトランジスタＱＨ１～ＱＨ３のゲートは水平走査回路ＨＳＲの各回路段に接続されている。水平走査回路ＨＳＲも、前記垂直走査回路ＶＳＲと同様に、シフトレジスタを備え、該シフトレジスタは水平初期化信号φＩＮＴＨにより全回路段のセットまたはリセットが可能なものが使用される。
【0008】図6の固体撮像装置は、例えば電子スチルカメラに使用された場合には、所定の露光時間の経過後に、垂直走査回路ＶＳＲに垂直スタート信号φＳＴＶを加え、かつ垂直シフト用クロック信号φＣＫＶを加えることにより、垂直走査回路ＶＳＲのシフトレジスタが順次前記スタート信号φＳＴＶを各回路段にシフトするよう動作する。これによって、各行ラインＧＶ１，ＧＶ２，ＧＶ３が順次選択される。各静電誘導トランジスタＱＳには入射光に応じた信号電荷が蓄積されており、選択された行においてはそのゲート電圧に所定の選択電圧が加えられることによって該静電誘導トランジスタがソースフォロアとして動作し蓄積された電荷に対応する電圧を各列ラインＬＶに出力する。すなわち、選択された行の静電誘導トランジスタＱＳからの信号が同時に各垂直読み出し線ＬＶに出力される。
【0009】そして、このとき転送信号φＴにより各列の転送トランジスタＱＴを導通させて信号電荷を容量ＣＴ１，ＣＴ２，ＣＴ３に充電した後にＱＴを遮断し、垂直走査回路ＨＳＲにより順次水平読み出しトランジスタＱＨをオンとして各列ごとの信号が水平出力線ＨＯＵＴに出力される。
【0010】ところで、このような固体撮像装置が、例えば電子スチルカメラに使用された場合には、シャッタを押した瞬間に全画素のリセットを行なった後被写体画像の撮像が行なわれる。図6の固体撮像装置においては全画素のリセットは次のようにして行なわれる。
【0011】すなわち、垂直走査回路ＶＳＲは、シフトレジスタを含み、初期化信号φＩＮＴＶ、クロック信号φＣＫＶ、走査開始信号φＳＴＶで制御される。初期化信号φＩＮＴＶとφＳＴＶをハイにすると垂直走査回路ＶＳＲの全回路段がプリセットされて全ての行ラインＧＶ１，ＧＶ２，ＧＶ３がハイになり、全ての画素が選択状態になる。これに対し、初期化信号φＩＮＴＶをハイにし、走査開始信号φＳＴＶをローにすると垂直走査回路ＶＳＲの各回路段がリセットされ、全画素が非選択状態になる。初期化信号φＩＮＴＶをローにすると垂直走査回路ＶＳＲが通常のシフト動作を開始し、スタート信号φＳＴＶがハイになった時点からクロック信号φＣＫＶが入るたびに順次各行ラインＧＶ１，ＧＶ２，ＧＶ３が順次高レベルとなって画素が1行ずつ順次選択され

る。

【００１２】そして、図６の固体撮像装置において全画素のリセットを行なうためには、まず垂直読み出し専用リセット信号φＲＳＴＶをハイにして、各列の垂直リセット用トランジスタＱＲＳＴＶ１～３をオンとし、各列ラインＬＶ１，ＬＶ２，ＬＶ３をグランドに接続する。

【００１３】次に、垂直走査回路ＶＳＲの前記初期化信号φＩＮＴＶと走査開始信号φＳＴＶを共にハイにして垂直走査回路ＶＳＲの各回路段をプリセット状態にする。これによって各行ラインＧＶ１，ＧＶ２，ＧＶ３が共にハイレベルとなって全画素の選択状態となる。この場合の各行ラインＧＶ１，ＧＶ２，ＧＶ３のハイレベルの電圧、すなわち制御信号φＳＲ１～３の電圧は、静電誘導トランジスタＱＳ１１～３３のリセット用電圧ＶＲＳＴＰとなるよう設定される。

【００１４】これによって、周知のように、各静電誘導トランジスタＱＳ１１～ＱＳ３３のゲート電極下部に反転層が形成されて該静電誘導トランジスタＱＳ１１～３３のソース・ドレイン間にチャネルができ、ゲートに充電されていた残存電荷が流れ出して全画素のリセットが行なわれる。このとき各画素の静電誘導トランジスタＱＳ１１～ＱＳ３３にはリセットによる残存電荷の流出による電流が同時に流れる。

【００１５】

【発明が解決しようとする課題】このように、従来の増幅型撮像素子を有する固体撮像装置においては、全画素のリセットを行なう場合には、全画素を同時に選択することにより、増幅手段を含む画素部を一体としてリセットを行なっていた。このため、リセット時に、各画素内の増幅手段も全て同時にオンになって、全増幅手段の電流が一斉に流れるようになっていた。このときの電流をラッシュ電流と言うが、個々の画素のラッシュ電流は小さくとも、全画素が同時にオンとなるため撮像装置全体では大きなラッシュ電流が流れる。

【００１６】例えば各画素のラッシュ電流が数マイクロアンペアであるとしても、画素数が１００万画素の場合には、撮像装置全体では数アンペアに達する。固体撮像装置のチップ内に数アンペアに達する電流が流れると、エレクトロマイグレーションによる信頼性の低下が問題になり、またチップ内の各部分の寄生インピーダンスによりチップ内各部分の電圧が所定の電圧範囲におさまりきらず、チップが固体撮像装置として期待した性能を発揮できず、あるいはラッシュ電流による誤動作などを生じる恐れもあった。

【００１７】したがって、本発明の目的は、このような従来の装置における問題点に鑑み、増幅型の画素を使用した固体撮像装置において、リセット時の過大なラッシュ電流を防止し、固体撮像装置のチップ全体が所定の性能を発揮できるようにすると共に、固体撮像装置の信頼性の低下をも的確に防止できるようにすることにある。

【００１８】

【課題を解決するための手段】上記目的を達成するため、本発明の第１の態様によれば、光電変換を行なう複数の画素と、前記複数の画素を順次選択して読み出すための走査回路を具備する固体撮像装置において、前記走査回路は複数の回路段が継続接続されて構成され所定の制御信号の入力に応じて前記複数の回路段の出力をほぼ同時に所定の論理状態に設定可能なシフトレジスタを備えたものとし、前記画素は各々少なくとも光信号に応じた信号電荷を蓄積する受光素子と、該受光素子に蓄積された信号電荷を増幅する増幅素子とを備えたものとし、かつ前記走査回路のシフトレジスタの複数の回路段の出力を前記所定の論理状態に設定することによって複数の画素を選択するとともに、選択した複数の画素において前記増幅素子をカットオフした状態で前記受光素子の電荷をリセットすることによりリセット時のラッシュ電流を低減する。

【００１９】このような構成では、前記走査回路のシフトレジスタによって複数の画素を選択し、かつ選択した複数の画素において前記増幅素子をカットオフした状態で前記受光素子の電荷をリセットする。したがって、リセット時に増幅素子にラッシュ電流が流れることはなくなり、多数の画素を有する固体撮像装置における全画素を同時にリセットしたとしても過大なラッシュ電流が流れることはなくなる。したがって、固体撮像装置の信頼性が低下することはなく、しかも固体撮像装置のチップ内の各部分の電圧がラッシュ電流によって大きな変動を起こすこともなくなり、固体撮像装置が本来の性能を的確に発揮できるようになる。

【００２０】この場合、前記各々の画素は、さらに、前記受光素子に蓄積された信号電荷を前記増幅素子の制御電極に転送する転送素子と、前記増幅素子の制御電極の電荷をリセットするリセット素子とを具備し、前記転送素子および前記リセット素子を共にオンとして受光素子の電荷をリセットするものとすることができる。

【００２１】このような画素構成をとることによって、リセット時には前記転送素子とリセット素子とを共にオンとし、かつリセット素子を介して増幅素子の制御電極に該増幅素子をカットオフする電圧を加えることにより、増幅素子をカットオフした状態で、受光素子に蓄積された電荷を前記転送素子およびリセット素子を介して放出することが可能になる。

【００２２】さらに、前記転送素子およびリセット素子を共にオンとして受光素子の電荷をリセットする際に、前記増幅素子にバイアス電圧を印加して前記増幅素子をカットオフ状態に保持するためのバイアス電圧印加手段を含むよう構成することもできる。

【００２３】この場合は、上記バイアス電圧印加手段によって画素のリセット時に前記増幅素子に対し、前記増幅素子をカットオフ状態にするためのバイアス電圧を印

加することができる。したがって、受光素子および増幅素子の特性をそれぞれ独立に最適のものに設定することができ、増幅素子を完全にカットオフした状態で受光素子の完全空乏化が達成でき、各素子の設計の自由度が増大し、高品質の固体撮像装置が実現できる。

【００２４】また、本発明の他の態様では、行および列方向に２次元状に配置され各々光信号に応じた信号電荷を蓄積し増幅する増幅型光電変換手段からなる複数の画素と、列方向に配列された各画素の出力端子を共通に接続した各列ライン毎に設けられた定電流回路と、前記画素を選択駆動する水平及び垂直各走査回路とを有する固体撮像装置において、前記垂直走査回路は複数の回路段が継続接続されて構成され所定の制御信号の入力に応じて前記複数の回路段の出力をほぼ同時に所定の論理状態に設定可能なシフトレジスタを備えたものとし、前記画素は各々光信号に応じた信号電荷を蓄積する受光素子と該受光素子に蓄積された信号電荷を増幅する増幅素子と前記受光素子に蓄積された信号電荷を前記増幅素子の制御電極に転送する転送素子と前記増幅素子の制御電極の電荷をリセットするリセット素子とを具備し、各行の画素の転送素子の制御電極は共通に対応する行ラインに接続され各行の行ラインは前記垂直走査回路の対応回路段に接続されすべての画素のリセット素子の制御電極は共通にリセット制御信号入力端子に接続され、かつ前記垂直走査回路のシフトレジスタの複数の回路段の出力を前記所定の論理状態に設定することによって前記各行ラインを介してすべての転送素子をオンとし、かつ前記リセット制御信号をすべての画素のリセット素子に加えることによって全画素のリセット素子をオンとし、受光素子の電荷を転送素子およびリセット素子を介してリセットするとともに、このリセットの際にオンとなったリセット素子を介して増幅素子の制御電極に該増幅素子をカットオフ状態とする電圧を印加することにより、リセット時のラッシュ電流を低減する。

【００２５】このような構成に係わる固体撮像装置においては、リセット時には、前記垂直走査回路のシフトレジスタの複数の回路段の出力を所定の論理状態とすることによって各行ラインの全ての転送素子をオンとし、かつ全ての画素のリセット素子をオンとし、受光素子の電荷を転送素子およびリセット素子を介してリセットすることができる。また、このリセットの際にオンとなったリセット素子を介して増幅素子の制御電極に該増幅素子をカットオフ状態とする電圧を印加しておけば、リセット時に増幅素子にラッシュ電流が流れることはなくなり、多数の画素を同時にリセットしても固体撮像装置全体として過大なラッシュ電流が流れることはなくなる。

【００２６】本発明のさらに他の態様では、行および列方向に２次元状に配置され各々光信号に応じた信号電荷を蓄積し増幅する増幅型光電変換手段からなる複数の画素と列方向に配列された各画素の出力端子を共通に接続した各列ライン毎に設けられた定電流回路と前記画素を選択駆動する水平及び垂直各走査回路とを有する固体撮像装置において、前記垂直走査回路は複数の回路段が継続接続されて構成され所定の制御信号の入力に応じて前記複数の回路段の出力をほぼ同時に所定の論理状態に設定可能なシフトレジスタを備えたものとし、前記画素は各々光信号に応じた信号電荷を蓄積する受光素子と該受光素子に蓄積された信号電荷を増幅する増幅素子と前記受光素子に蓄積された信号電荷を前記増幅素子の制御電極に転送する転送素子と前記増幅素子の制御電極の電荷をリセットするリセット素子とを具備し、各行の画素の転送素子の制御電極は共通に対応する行ラインに接続され各行の行ラインは前記垂直走査回路の対応回路段に接続されすべての画素のリセット素子の制御電極は共通にリセット制御信号入力端子に接続され、また各列ラインは各列ラインに接続された画素の増幅素子をカットオフ状態にするために各列ラインを介して増幅素子にバイアス電圧を印加する手段を備え、かつ前記垂直走査回路のシフトレジスタの複数の回路段の出力を前記所定の論理状態に設定することによって前記各行ラインを介してすべての転送素子をオンとし、かつ前記リセット制御信号をすべての画素のリセット素子に加えることによって全画素のリセット素子をオンとし、受光素子の電荷を転送素子およびリセット素子を介してリセットするとともに、このリセットの際に前記バイアス電圧印加手段によって全画素の増幅素子をカットオフ状態とすることにより、リセット時のラッシュ電流を低減する。

【００２７】この場合も、垂直走査回路のシフトレジスタの複数の回路段の出力を所定の論理状態に設定することによって各行ラインを介して全ての転送素子をオンとし、かつ前記リセット制御信号によって全ての画素のリセット素子をオンとすることにより、受光素子の電荷を転送素子およびリセット素子を介して放出することができる。そして、このリセットの際に、前記バイアス電圧印加手段によって全画素の増幅素子をカットオフ状態とすることにより、リセット時のラッシュ電流を低減できる。前記バイアス電圧印加手段は、画素の増幅素子に他の素子とは独立に所望の適切なバイアス電圧を印加することができるから、画素の各素子の設計の自由度を増大させることができる。すなわち、前記転送素子およびリセット素子を介して受光素子が完全に空乏化される電圧を供給することができ、一方前記増幅素子には該増幅素子を充分にカットオフ状態とするバイアス電圧を独立に印加することができ、受光素子と増幅素子をそれぞれ所望の最適の特性を有するよう設計することができる。

【００２８】

【発明の実施の形態】図１は、本発明に係わる固体撮像装置の概略の構成を示すブロック図であり、２次元のイメージセンサの例を示している。同図の固体撮像装置は、複数の画素１を有する画素部３と、垂直走査回路５

と、水平読み出し部7と、水平走査回路9とを備えている。

【0029】画素部3は、それぞれ後に詳細に説明するように受光用のフォトダイオードおよび増幅素子などを備えた画素1がマトリクス状に配置されて構成されている。垂直走査回路5は、画素部3の1水平ライン（行ライン）分の画素を順次選択するものであり、後に示す構造のダイナミックシフトレジスタで構成される。水平読み出し部7は、画素部3から1水平ライン分の画素の電荷を受け入れ、これを水平走査回路9からの走査パルスに基づき順次出力するものである。水平走査回路9も前記垂直捜査回路5と同様のダイナミックシフトレジスタによって構成される。

【0030】垂直走査回路5に入力されている信号φSTVは垂直スタートパルスであり、ダイナミックシフトレジスタの初期入力データとなる。また垂直走査回路5には、そのダイナミックシフトレジスタのシフトを行なうための垂直クロックパルスφCKVおよび垂直初期化パルスφINTVが入力される。

【0031】また、水平走査回路9に入力されている信号φSTHは水平走査回路9を構成するダイナミックシフトレジスタのスタート信号であり、φCKHは水平シフト用のクロック信号である。また、水平走査回路9には必要に応じて該水平走査回路9を構成するダイナミックシフトレジスタを初期化するための水平初期化パルスφINTHが入力される。

【0032】図1の固体撮像装置では、例えばスチルビデオカメラなどに使用された場合、シャッタを押す前には固体撮像装置は擬似動作をさせておく、すなわち走査はするが出力信号は使用しない状態としておく。そして、シャッタが押されたら、垂直走査回路5に10マイクロ秒程度の一定期間初期化パルスφINTVを加え、同時にスタートパルスφSTVをHレベルにすると、擬似動作中の垂直走査回路5のシフトレジスタの全段が強制的にプリセット状態になって全画素が選択状態になり全画素の電荷がリセットできる。

【0033】次に、垂直スタートパルスφSTVをLレベルにして垂直走査回路5をリセット状態とし、かつ水平走査回路9にも初期化パルスφINTHを加えかつ水平スタートパルスφSTHをLレベルにして水平走査回路9をリセット状態にした後に、通常動作に戻って各シフトレジスタのシフト動作を開始する。このとき各画素は画像情報の蓄積を開始しており、所定の露光時間の経過後再度初期化パルスφINTV，φINTHをHレベル、垂直スタートパルスφSTVと水平スタートパルスφSTHをLレベルにして各シフトレジスタを強制リセットした後に通常の動作に戻って読出し動作を開始すると、所定の時間露光された映像信号を得ることができる。

【0034】なお、図1の固体撮像装置では、通常の読み出し動作は、垂直走査回路5および水平走査回路9の各初期化パルスφINTVおよびφINTHをそれぞれ低レベルとした状態で、垂直走査回路5において例えば高レベルのスタート信号φSTVをクロック信号φCKVで順次シフトし、画素部3の1水平ライン分の画素を順次選択する。選択された1水平ライン分の各画素のフォトダイオードに蓄積されていた電荷は水平読み出し部7に転送される。次に、水平走査回路9により例えば高レベルのスタート信号φSTHをクロック信号φCKHにより順次シフトすることにより、該水平走査回路9によって水平読み出し部7に転送された電荷を1画素分だけ順次水平方向に転送し出力端子から外部に読み出す。

【0035】図2は、図1の固体撮像装置の詳細な回路構成を示す。図2の固体撮像装置において、図1と同じ部分は同じ参照数字で示されている。すなわち図2の固体撮像装置も複数の画素1を備えた画素部3と、垂直走査回路5と、水平読み出し部7と水平走査回路9などによって構成されている。図2の回路では、説明の簡略化のため画素部3は3行×3列の画素1から構成されるものとしている。

【0036】各画素1は受光素子であるフォトダイオードPD、接合型電界効果トランジスタ（JFET）からなる増幅素子QA、フォトダイオードPDの電荷を増幅素子QAのゲートに転送するためのMOSトランジスタからなる転送用スイッチQT、増幅素子QAのゲート電極を所定の電圧に設定するためのMOSトランジスタからなるリセットスイッチQRSTから構成されている。なお、図面では、各素子に添字がされているが、説明の簡略化のため同じ種類の素子を代表して表現する場合には添字は省略することがある。図2に示される各画素1においては、受光手段であるフォトダイオードPDと増幅素子QAのゲートが構造上分離されている。

【0037】各画素1の増幅素子QAのうち、垂直方向に配置された画素の増幅素子QAのソースは各列の列ラインLV（LV1～LV3）を介してそれぞれの列の定電流源CSVに接続されている。各定電流源CSVは増幅素子QAをソースフォロアとして動作させたときの負荷となる。各定電流源CSVの他端は共通に所定の電源VEEに接続されている。

【0038】各画素1のフォトダイオードPDのカソードは共通に所定の電源VDDに接続され、アノードは転送用スイッチQTのソースに接続されている。転送用スイッチQTのドレインは増幅素子QAのゲートおよびリセットスイッチQRSTのソースに接続されている。各増幅素子QAのソースは列ごとに共通にそれぞれの列ラインLV（LV1～LV3）に接続されている。各転送用スイッチQTのゲートは行ごとに共通に垂直走査回路5に接続され第1の垂直走査信号φTRを受けるよう構成されている。各行の垂直走査信号φTR1～φTR3は垂直走査回路5のそれぞれの回路段の出力に接続され

ている。リセットスイッチQRSTのゲートは全画素共通に制御信号φPGに接続され、ドレインは水平方向に共通に垂直走査回路5に接続されてそれぞれの行ごとに第2の垂直走査信号φRDが供給されるよう構成されている。各増幅素子QAのドレインは共通に前記フォトダイオードPDのアノードと同じ電源VDDに接続されている。

【0039】なお、垂直走査回路5の各回路段の出力は、それぞれ異なった電圧レベルの第1および第2の垂直走査信号φTRおよびφRDを供給するため、例えば、シフトレジスタの各回路段の出力にそれぞれ所定の電圧シフト回路を接続して構成することもできる。

【0040】水平読み出し部7は、各列ごとに読み出しゲートトランジスタQTC、容量CTおよび水平読み出し用のスイッチ素子QHで構成される。各列ラインLVの上端は読み出しゲートトランジスタQTCのドレインに接続され、該読み出しゲートトランジスタQTCのソースはそれぞれの列の水平読み出し用スイッチ素子QHのドレイン、および容量CTに接続されている。容量CTの他端は接地されている。全ての読み出しゲートトランジスタQTCのゲートは共通に接続され転送パルスφTが供給できるよう構成されている。また、水平読み出し用スイッチ素子QHのゲートは各列ごとに水平走査回路9のシフトレジスタの各回路段の出力に接続されている。さらに、水平読み出し用スイッチ素子QHのソースは共通に水平出力線HOUTを介してビデオ出力端子に接続されている。

【0041】以上のような構成を有する固体撮像装置において画素のリセットは次のように行なう。すなわち、垂直走査回路5の初期化パルスφINTVおよびスタートパルスφSTVを共にハイにして垂直走査回路5の全回路段をプリセットして全画素の選択状態とする。これによって、全回路段の第1の垂直走査信号φTR（φTR1～φTR3）を全て同時にハイにして全画素の転送用スイッチQTをオンとする。また、全画素共通のリセット制御信号φPGを加えて全画素のリセットスイッチQRSTをオンにする。

【0042】このとき第2の垂直走査信号φRD（φRD1～φRD3）の電圧は各画素の増幅素子QAを構成するJFETがカットオフする電圧VGLとする。

【0043】このようにすると、各画素のフォトダイオードPDに蓄積されていた残留電荷は、転送素子QTとリセット素子QRSTを通じて排出され、フォトダイオードPDは完全空乏化されてリセットされる。そして、この場合増幅素子QAのゲート電圧は前述のようにVGLでありしたがって該増幅素子QAはカットオフしているので、該増幅素子QAには電流が流れない。すなわち、フォトダイオードPDに流れる電流が増幅素子QAによって増幅されて増幅された電流が流れることはない。このため、各画素のラッシュ電流がきわめて小さくなり、固体撮像装置全体として過大なラッシュ電流が流れることはなくなる。

【0044】なお、図2の固体撮像装置において信号の読み出しを行なう場合は、垂直走査回路5の初期化パルスφINTVをローレベルとし、スタートパルスφSTVをハイにすると共にクロック信号φCKVを加えて垂直走査回路5のシフト動作を行なわせる。これによって、各行の画素を順次選択し、選択された画素に蓄積されている信号を垂直読み出し線LVに出力する。そして、各列ラインに接続された読み出しゲートトランジスタQTCを転送パルスφTによってオンとし信号の読み出し電荷をそれぞれの列の容量CTに充電する。また、水平走査回路9においても、初期化パルスφINTHをローレベル、スタートパルスφSTHをハイレベルとしかつクロック信号φCKHを加えることによりシフト動作を行なわせる。これによって、各列の水平読み出し用スイッチ素子QHが順次オンとされて各列の読み出し信号が水平出力ラインHOUTに供給されビデオ出力端子から外部に出力される。

【0045】また、このような信号の読み出しを行なう場合には、リセット制御信号φPGにより全画素のリセット素子QRSTをオンにする。そして、選択された行に対しては第2の垂直走査信号φRDの電圧を各画素の増幅素子QAがオンになって活性化する電圧VGHとし、非選択画素に対しては増幅素子QAがカットオフする前記電圧VGLとする。この状態で、前記制御信号φPGをオフにしても増幅素子QAのゲート浮遊容量により該増幅素子QAのゲート電圧は同じ値に保持される。したがって、リセット制御信号φPGにより全画素のリセット素子QRSTをオフにした後に、第1の垂直走査信号φTRにより選択された行の画素の転送素子をオンにする。これによって、フォトダイオードPDに蓄積されていた信号電荷が増幅素子QAのゲートに転送され該増幅素子QAのゲート電圧が信号に対応して変化する。この電圧を増幅素子QAをソースフォロアとして動作させて列ラインLVに出力し、前述のように水平走査回路9を走査して順次外部に読み出す。

【0046】図3は、本発明に係わる固体撮像装置の水平走査回路および垂直走査回路に使用可能なダイナミックシフトレジスタの構成を示す。図3のダイナミックシフトレジスタは、CMOSプロセスを使用して作成され、クロックパルスによって順次活性化されるいわゆるクロックドインバータを使用した例を示している。

【0047】図3のダイナミックシフトレジスタにおいては、例えば正の電源電圧V_{DD}と負の電源電圧V_{SS}との間に直列接続された2個のPMOSトランジスタP1およびP2と2個のNMOSトランジスタN2およびN1とによって1段のクロックドインバータを構成している。PMOSトランジスタP3，P4およびNMOSトランジスタN4，N3が2段目のクロックドインバー

タを構成し、PMOSトランジスタP5，P6と2個のNMOSトランジスタN6，N5とが3段目のクロックドインバータを構成し、2個のPMOSトランジスタP7，P8と2個のNMOSトランジスタN8とN7とが4段目のクロックドインバータを構成し、以下同様である。

【0048】各回路段のクロックドインバータにおいて中央に位置するPMOSトランジスタとNMOSトランジスタ、例えば1段目ではP2とN2、2段目ではP4とN4、3段目ではP6とN6、4段目ではP8とN8、はそれぞれCMOSインバータを構成している。各CMOSインバータと電源V_{DD}およびV_{SS}との間に接続されたトランジスタはこれらのCMOSインバータを活性化させるための制御用トランジスタである。

【0049】これらの制御用トランジスタのうちPMOSトランジスタP1，P5，…のゲートは内部クロック信号線CP1に接続され、PMOSトランジスタP3，P7，…のゲートは内部クロック信号線CP2に接続されている。また、他の導電形の制御用トランジスタ、すなわちNMOSトランジスタN1，N5，…のゲートは内部クロック信号線CN1に接続され、NMOSトランジスタN3，N7，…のゲートは他の内部クロック信号線CN2に接続されている。

【0050】また、1段目のCMOSインバータを構成する各トランジスタP2およびN2のゲートにはスタートパルスφSTが供給される。1段目のCMOSインバータの出力は2段目のCMOSインバータの入力、すなわちトランジスタP4およびトランジスタN4のゲートに接続され、2段目のCMOSインバータの出力は3段目のCMOSインバータの出力に接続され、3段目のCMOSインバータの出力は4段目のCMOSインバータの入力に順次接続されている。

【0051】図3のダイナミックシフトレジスタはさらに、同時活性化回路を構成するインバータINV2、ORゲートOR1，OR2を備え、さらに2個のインバータINV3，INV4を備えている。ORゲートOR1およびOR2のそれぞれの一方の入力には初期化パルスφINTが供給される。ORゲートOR1の他方の入力はクロックパルスφCKが供給され、他のORゲートOR2の他方の入力はクロックパルスφCKをインバータINV2で反転した信号が供給される。ORゲートOR1の出力は前記内部クロック信号線CN2に接続され、かつインバータINV4を介して内部クロック信号線CP2に接続されている。ORゲートOR2の出力は内部クロック信号線CN1に接続され、かつインバータINV3を介して内部クロック信号線CP1に接続されている。

【0052】以上のような構成を有するダイナミックシフトレジスタにおいては、初期化パルスφINTがロー（L）レベルの場合はORゲートOR1の出力にはクロックパルスφCKが発生し、ORゲートOR2の出力にはクロックパルスφCKを反転したクロックパルスが供給される。したがって、クロックパルスφCKがハイ（H）レベルのときは、内部クロック信号線CN2がHレベル、内部クロック信号線CP2がLレベルとなり、トランジスタP3，P7，…およびN3，N7，…がオンとなる。これに対し、クロック信号φCKがLレベルの場合は、ORゲートOR2の出力がHレベルとなりトランジスタP1，P5，…およびN1，N5，…がオンとなる。したがって、クロック信号φCKによって各回路段の第1のインバータと第2のインバータとが交互に活性化され、スタートパルスφSTが順次後続の回路段へとシフトされる。

【0053】これに対し、初期化パルスφINTをHレベルにすると、クロックパルスφCKのレベル如何にかかわらず、ORゲートOR1およびOR2の出力は共にHレベルとなる。したがって、内部クロック信号線CN1，CN2は共にHレベルとなり、内部クロック信号線CP1，CP2は共にLレベルとなる。このため、全てのクロックドインバータの制御用トランジスタP1，P3，P5，P7，…およびN1，N3，N5，N7，…が同時にオンとなる。すなわち、全てのクロックドインバータが同時に活性化される。

【0054】これによって、クロックパルスφCKとは無関係に入力信号φSTが各インバータで反転されて高速度で後段の回路に伝達される。したがってスタートパルスφSTをLレベルにすれば、全ての回路段の出力S1，S2，…も全てLレベルとなり、スタートパルスφSTをHレベルとすれば全ての回路段の出力S1，S2，…はHレベルとなる。すなわち、ほぼ瞬時的に全回路段あるいは所望の回路段までの出力をセットあるいはプリセットすることができる。また、回路は全て活性状態にあるから、リセットまたはプリセット状態を安定して長時間継続することも可能である。なお、通常の固体撮像装置に使用されるクロックドインバータの遅延時間は、通常数ナノ秒以下であり、仮にクロックドインバータが1000段あったとしても入力段から最終段まで数マイクロ秒以下でデータの伝達が可能であり、ほぼ瞬時に各回路段のリセットあるいはプリセットを行なうことができる。

【0055】図4は、本発明の固体撮像装置に使用できるダイナミックシフトレジスタの他の構成例を示す。図4のダイナミックシフトレジスタは、各回路段ごとに2個のCMOSインバータを備えている。すなわち、第1の回路段はPMOSトランジスタP11とNMOSトランジスタN11からなる第1のCMOSインバータと、PMOSトランジスタP12およびNMOSトランジスタN12からなる第2のCMOSインバータとを有している。第2の回路段は、PMOSトランジスタP13およびNMOSトランジスタN13からなる第1のCMO

Sインバータと、PMOSトランジスタP14およびNMOSトランジスタN14からなる第2のCMOSインバータとを備えており、以下同様である。各インバータは伝達ゲートを介して順次縦続接続されている。すなわち、トランジスタP11およびN11からなるインバータの出力は第1の伝達ゲートT1を介してトランジスタP12およびN12からなるインバータの入力に接続されており、トランジスタP12，N12からなるインバータの出力は第2の伝達ゲートT2を介してトランジスタP13，N13からなるインバータの入力に接続されており、トランジスタP13，N13からなるインバータの出力は第3の伝達ゲートT3を介してトランジスタP14，N14からなるインバータの入力に接続され、以下同様である。

【0056】伝達ゲートT1，T3，…のPMOSトランジスタ側のゲートは内部クロック信号線CP1に接続され、NMOSトランジスタのゲートは内部クロック信号線CN1に接続されている。また、伝達ゲートT2，T4，…のPMOSトランジスタのゲートは内部クロック線CP2に接続され、NMOSトランジスタのゲートは内部クロック信号線CN2に接続されている。

【0057】図4のダイナミックシフトレジスタは、図3のものと同様に、インバータINV2、ORゲートOR1，OR2からなる同時活性化回路を備えており、またORゲートOR1，OR2の出力をそれぞれ反転して内部クロック信号線CP2，CP1に供給するインバータINV4，INV3を備えている。ORゲートOR1，OR2の出力はまた内部クロック信号線CN2，CN1に接続されている。

【0058】図4のダイナミックシフトレジスタにおいては、初期化パルスφINTがLレベルの場合には、ORゲートOR1およびOR2の出力はそれぞれクロックパルスφCKおよび該クロックパルスφCKを反転した反転クロックパルスが出力される。これらのクロックパルスφCKおよびその反転クロックパルスがそれぞれ内部クロック信号線CN2およびCN1に供給される。また、ORゲートOR1，OR2からそれぞれ出力されるクロックパルスφCKおよびその反転クロックパルスがそれぞれさらにインバータINV4，INV3によって反転されてそれぞれ内部クロック信号線CP2，CP1に供給される。すなわち内部クロック信号線CP2にはクロック信号φCKを反転したクロックパルスが、内部クロック信号線CP1にはクロックパルスφCKが供給される。

【0059】したがって、クロックパルスφCKがHレベルの場合は、伝達ゲートT2，T4，…が導通し、クロックパルスφCKがLレベルの場合は伝達ゲートT1，T3，…が導通する。すなわちクロック信号φCKによって伝達ゲートT1，T2，T3，T4，…が交互に導通、非導通とされる。これによって、スタートパルスφSTが、周知のごとく、順次後続の回路段へと伝達されシフト動作が行なわれる。

【0060】これに対し、初期化パルスφINTがHレベルの場合は、ORゲートOR1，OR2の出力は共に、クロックパルスφCKのレベルにかかわらず、Hレベルとなる。このため、内部クロック信号線CN1，CN2は共にHレベル、内部クロック信号線CP1，CP2は共にLレベルとなり、全ての伝達ゲートT1，T2，T3，T4，…が導通する。すなわち、全ての回路段のインバータが直接縦続接続されることになる。したがって、スタートパルスφSTが順次反転されながら各インバータによって直接伝達される。したがって、図4の回路においても各回路段を瞬時にリセットあるいはプリセットすることが可能になる。

【0061】なお、上述の説明においては、ダイナミックシフトレジスタとして2種類のものにつき説明したが、本発明には種々の形式のダイナミックシフトレジスタを使用できることは明らかである。すなわち、各回路段が2段1組のダイナミック形インバータ回路で構成されており、片方が実質的に活性状態のとき、他方は実質的に不活性状態として入力信号を順次後続の回路段に伝達する形式のダイナミックシフトレジスタであれば本発明は適用できる。これらの場合、2段1組のダイナミック形インバータを同時に活性化し、複数回路段にわたり入力信号を直接後続の回路段に伝達し、リセットやプリセットを強制的に瞬時に行なわせることができる。

【0062】次に、図5は、本発明の別の実施態様に係わる固体撮像装置の回路構成を示す。図5においても前記図1と同じ部分は同じ参照数字で示されている。また、図5の固体撮像装置では、前記図2の固体撮像装置における各列ラインLV1，LV2，LV3がそれぞれプルアップ用のMOSトランジスタなどで構成されるスイッチ素子QPU1，QPU2，QPU3を介して所定のバイアス電圧VPUに接続されている。各スイッチ素子QPU1，QPU2，QPU3のゲートは共通に接続され所定の制御信号φPUが供給できるよう構成されている。また、バイアス電圧VPUは増幅素子QAのゲートが増幅素子QAの読み出し電圧VGHであっても該増幅素子QAがカットオフする電圧とされる。その他の部分は図2の回路と同じであり、同じ部分には同じ参照数字および参照符号が付されている。

【0063】図5の固体撮像装置において画素のリセットを行なう場合には、図2の場合と同様に、垂直走査回路5の全段をプリセットし、第1の垂直走査回路φTR1～TR3を全画素の転送用スイッチQTに加えて該転送用スイッチQTをオンとする。また制御信号φPGを加えて全画素のリセットスイッチQRSTをオンにする。このとき、第2の垂直走査信号φRD1～φRD3の電圧は各画素部の増幅素子QAの読み出し電圧VGHとする。

【0064】さらに、このとき、制御信号φPUにより各列のプルアップ用スイッチ素子QPUをオンとして各列ラインLV1～LV3を前記バイアス電圧VPUにバイアスする。このバイアス電圧VPUは、前述のように、増幅素子QAのゲートが読み出し電圧VGHであっても増幅素子QAがカットオフする電圧とする。これによって、増幅素子QAをカットオフした状態でフォトダイオードPDの残留電荷を転送素子QTおよびリセット素子QRSTを介して放出し、画素のリセットが行なわれる。そして、この場合フォトダイオードPDは増幅素子QAの読み出し電圧VGHに逆バイアスされた状態にリセットされる。しかしながら、プルアップ用のスイッチ素子QPUによって、各増幅素子QAのソース電圧が前記バイアス電圧VPUになっており、増幅素子QAには電流が流れない。すなわち、リセット時の過大なラッシュ電流が防止できる。なお、信号の読み出しを行なう場合は、プルアップ用のスイッチ素子QPUをカットオフとした状態で前記図2の固体撮像装置の場合と同様に行なう。

【0065】上記図2および図5の固体撮像装置において、各画素の受光素子の特性としては、リセット時に完全空乏化されるよう構成することが望ましい。しかしながら、そのような受光素子を構成するよう製造プロセス条件を設定すると、増幅素子QAを構成するJFETの特性が充分でない場合があり、逆にJFETの特性を重視すると受光素子の完全空乏化が達成できないことがある。したがって、受光素子のフォトダイオードと増幅素子のJFET特性が共に所望の特性に両立できる場合には、前記図2の構成とするのが望ましく、両立が困難または不可能な場合には図5の構成とするのが望ましい。

【0066】

【実施例】なお、上記図2および図5における固体撮像装置において、各電源および信号の電圧は具体的には次のように設定して高結果が得られる。すなわち電源電圧VDD＝5V、VEE＝0Vの条件で、前記各画素の増幅素子QAがオンになって活性化する読み出し電圧VGH＝－1Vとする。そして、前記図2の構成における、リセット時に各画素のリセット素子のドレインに供給される第2の垂直走査信号φRDの電圧VGLは例えば－3Vでよい。また、前記図5の構成における各画素をカットオフするためのバイアス電圧VPUは増幅素子QAのゲート電圧がVGH＝－1Vであっても該増幅素子QAがカットオフする電圧、例えば＋1V以上とする。

【0067】

【発明の効果】以上のように、本発明によれば、固体撮像装置において、リセットを行なう場合に各画素の増幅素子をカットオフした状態で受光素子のリセットを行なうよう構成したから、多数の画素を含む固体撮像装置におい全画素を同時にリセットする場合にも過大なラッシュ電流が発生することを防止できる。したがって、ラッシュ電流による固体撮像装置の信頼性の低下が防止できると共に、ラッシュ電流によるチップ内各部の電圧変動によって固体撮像装置に悪影響を与えることが防止され、固体撮像装置が本来の性能を発揮することが可能になる。このような固体撮像装置は、例えばシャッタを切った瞬間に全画素同時リセットが必要な電子スチルカメラなどに使用して好結果を得ることができる。

【図面の簡単な説明】

【図1】本発明に係わる固体撮像素子の概略の構成を示すブロック図である。

【図2】本発明の第1の実施形態に係わる固体撮像装置の詳細な構成を示す電気回路図である。

【図3】本発明に係わる固体撮像装置の走査回路に使用可能なシフトレジスタの構成を示す電気回路図である。

【図4】本発明に係わる固体撮像素子の走査回路に使用可能なシフトレジスタの他の構成を示す電気回路図である。

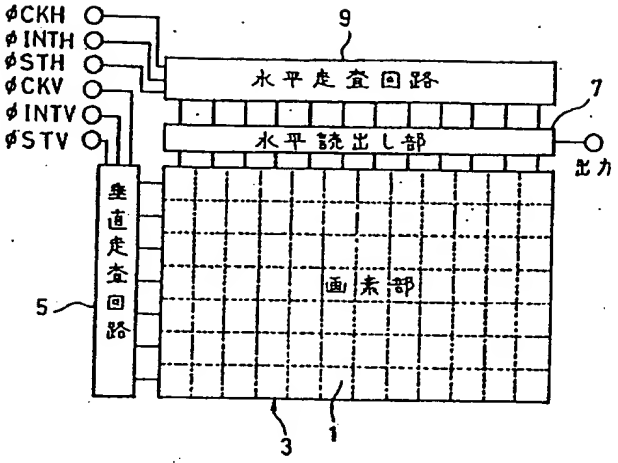
【図5】本発明の第2の実施形態に係わる固体撮像素子の詳細な構成を示す電気回路図である。

【図6】従来の固体撮像装置の構成を示す電気回路図である。

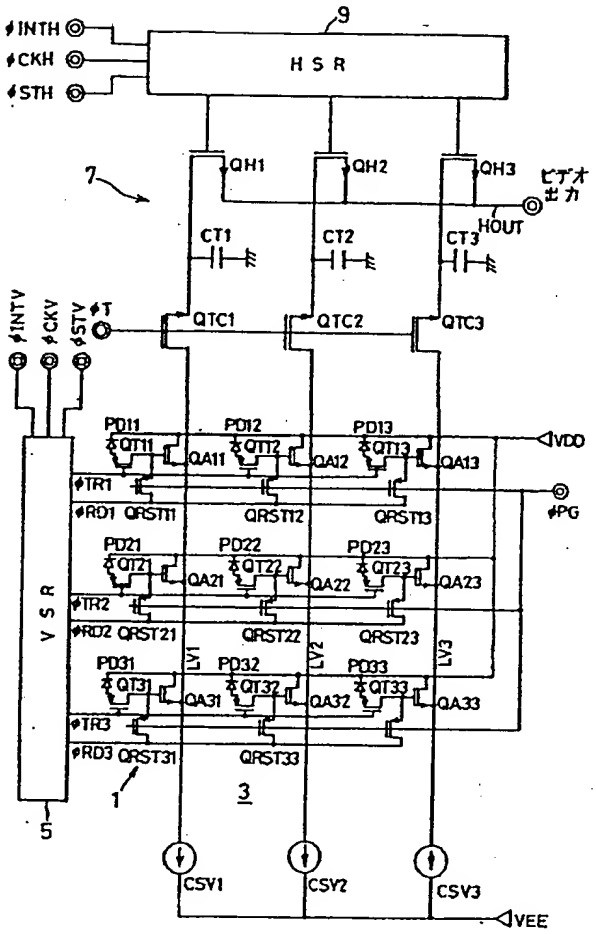
【符号の説明】

1　画素
3　画素部
5　垂直走査回路（VSR）
7　水平読み出し部
9　水平走査回路（HSR）
PD11，…，PD33　フォトダイオード
QT11，…，QT33　転送素子
QA11，…，QA33　増幅素子
QRST11，…，QRST33　リセット素子
CSV1，…，CSV3　定電流源
QTC1，…，QTC3　読み出しゲートトランジスタ
CT1，…，CT3　蓄積用容量
QH1，…，QH3　水平読み出し用スイッチ素子
QPU1，…，QPU3　プルアップ用スイッチ素子

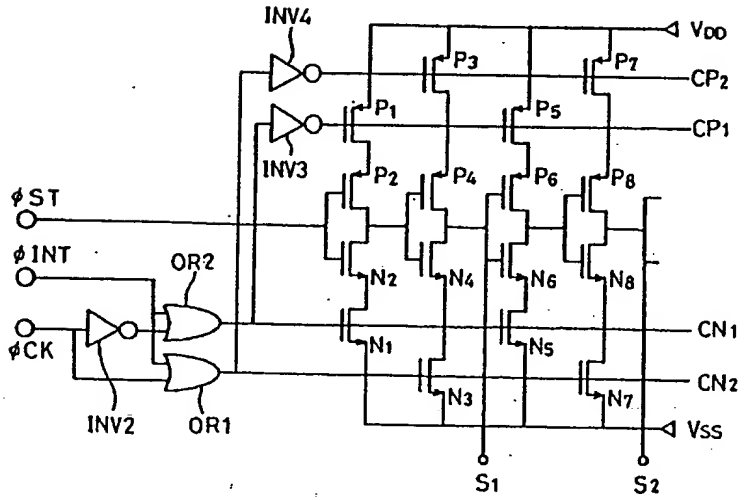
【図1】


φCKH
φINTH
φSTH
φCKV
φINTV
φSTV
9
水平走査回路
7
水平読出し部
出力
垂直走査回路
5
画素部
3
1

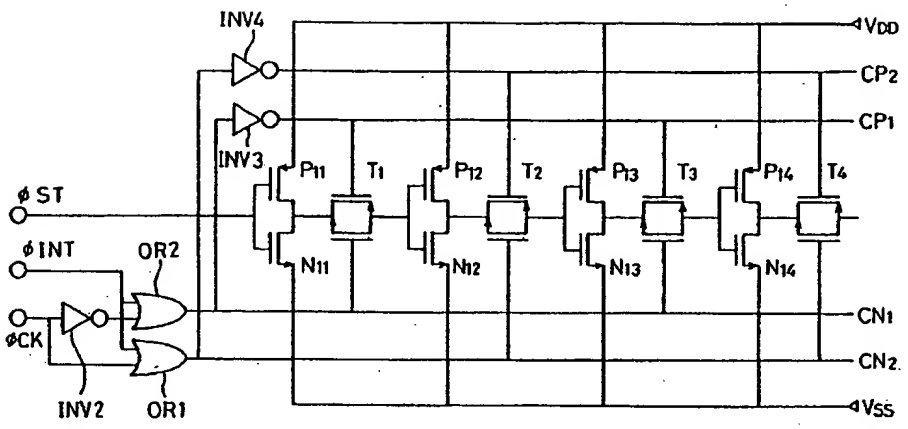
【図2】


φINTH
φCKH
φSTH
9
HSR
7
QH1
QH2
QH3
ビデオ出力
HOUT
CT1
CT2
CT3
φINTV
φCKV
φSTV
φT
QTC1
QTC2
QTC3
PD11
PD12
PD13
VDD
QT11
QT12
QT13
QA11
QA12
QA13
φTR1
φRD1
QRST11
QRST12
QRST13
φPG
PD21
PD22
PD23
QT21
QT22
QT23
QA21
QA22
QA23
φTR2
φRD2
QRST21
QRST22
QRST23
VSR
LV1
LV2
LV3
PD31
PD32
PD33
QT31
QT32
QT33
QA31
QA32
QA33
φTR3
φRD3
QRST31
QRST33
1
3
5
CSV1
CSV2
CSV3
VEE

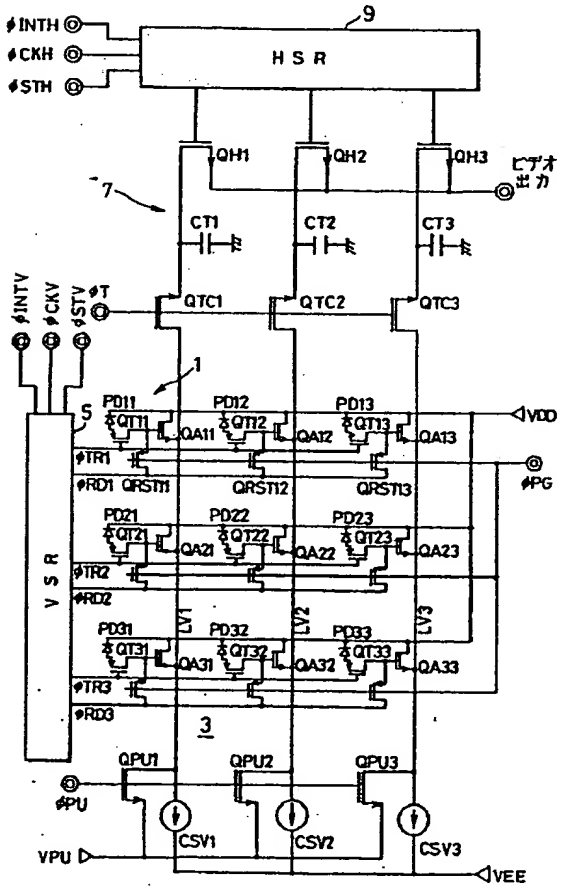
【図3】


INV4
VDD
P3
P7
CP2
P1
P5
CP1
INV3
P2
P4
P6
P8
φST
φINT
OR2
N2
N4
N6
N8
φCK
N1
N5
CN1
CN2
N3
N7
INV2
OR1
VSS
S1
S2

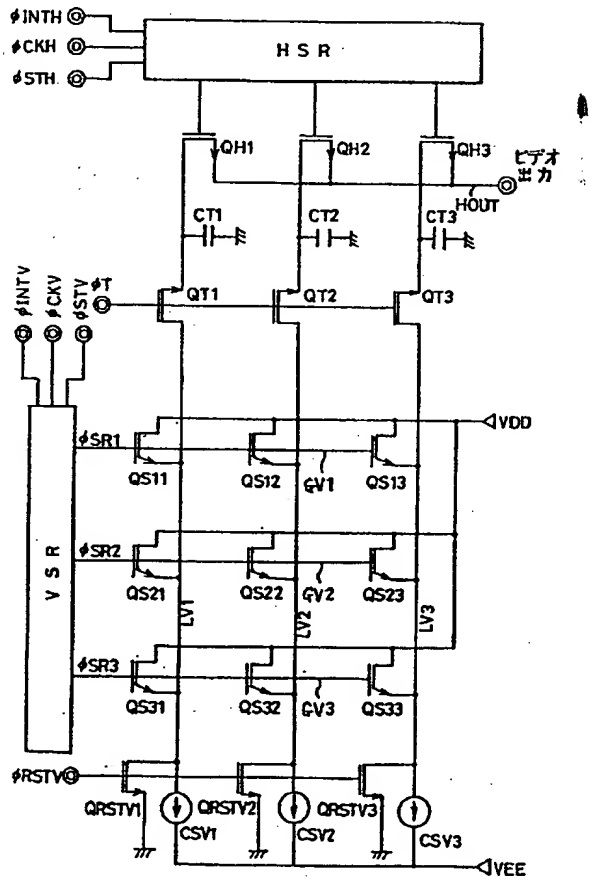
【図4】


INV4
INV3
INV2
OR2
OR1
φST
φINT
φCK
P11
T1
P12
T2
P13
T3
P14
T4
N11
N12
N13
N14
VDD
CP2
CP1
CN1
CN2
VSS

【図5】


φINTH
φCKH
φSTH
H S R
9
QH1
QH2
QH3
ビデオ出力
7
CT1
CT2
CT3
φINTV
φCKV
φSTV
φT
QTC1
QTC2
QTC3
1
5
PD11
PD12
PD13
QT11
QT12
QT13
QA11
QA12
QA13
VDD
φTR1
φRD1
QRST11
QRST12
QRST13
φPG
PD21
PD22
PD23
QT21
QT22
QT23
QA21
QA22
QA23
φTR2
φRD2
PD31
PD32
PD33
QT31
QT32
QT33
QA31
QA32
QA33
φTR3
φRD3
LV1
LV2
LV3
V S R
3
QPU1
QPU2
QPU3
φPU
VPU
CSV1
CSV2
CSV3
VEE

【図6】


φINTH
φCKH
φSTH
H S R
QH1
QH2
QH3
ビデオ出力
HOUT
CT1
CT2
CT3
φINTV
φCKV
φSTV
φT
QT1
QT2
QT3
VDD
φSR1
QS11
QS12
GV1
QS13
φSR2
QS21
QS22
GV2
QS23
LV1
LV2
LV3
V S R
φSR3
QS31
QS32
GV3
QS33
φRSTV
QRSTV1
QRSTV2
QRSTV3
CSV1
CSV2
CSV3
VEE